FSC-BT3131

Bluetooth 5.3 Wireless MCU Module Datasheet

Version 1.0

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Revision History

Version	Data	Notes	
1.0	2023/07/05	Initial Version	Stanley

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Contents

1. INTRODUCTION

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Overview

FSC-BT3131 is a wireless microcontroller (MCU) mainly focus on Bluetooth 5.3 low energy applications.

Very low active RF and MCU current and low-power mode current consumption provide excellent battery lifetime and allow for operation on small coin cell batteries and in energy-harvesting applications.

FSC-BT3131 contains a ARM® Cortex®-M0+ core that runs at 48 MHz as the main processor and a rich peripheral feature set that includes a unique ultra-low power sensor controller. This sensor controller is ideal for interfacing external sensors and for collecting analog and digital data autonomously while the rest of the system is in sleep mode. Thus, FSC-BT3131 is great for a wide range of applications where long battery lifetime, small form factor, and ease of use is important.

It supports GAP, ATT/GATT, SMP, L2CAP profiles. It integrates Baseband controller in a small package (Integrated chip antenna), so the designers can have better flexibilities for the product shapes.

Features

- 2.4-GHz RF Transceiver Compatible With Bluetooth low energy (BLE) 5.3 Specifications
- Link Budget of 102 dB for BLE
- Integrate MCU to execute Bluetooth protocol stack.
- Postage stamp sized form factor,
- Low power
- Class 1.5 support (up to +7 dBm)
- The default UART Baud rate up to 3Mbps
- UART, I^2C,SPI interfaces.
- Support the OTA upgrade.
- Bluetooth stack profiles support: LE HID, and all BLE protocols.

Application

- Home and Building Automation
  - – Connected Appliances
  - – Lighting
  - – Locks
  - – Gateways
  - – Security Systems
- Industrial
  - – Logistics
  - – Production and Manufacturing Automation
  - – Asset Tracking and Management
  - – HMI and Remote Display
  - – Access Control
- Retail
  - – Beacons
  - – Advertising
  - – ESL and Price Tags
  - – Point of Sales and Payment Systems
- Health and Medical
  - – Thermometers
  - – SpO2
  - – Blood Glucose and Pressure Meters
  - – Weight Scales
  - – Hearing Aids
- Sports and Fitness
  - – Activity Monitors and Fitness Trackers
  - – Heart Rate Monitors
  - – Running and Biking Sensors
  - – Sports Watches
  - – Gym Equipment
  - – Team Sports Equipment
- HID
  - – Voice Remote Controls
  - – Gaming
  - – Keyboards and Mice

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Module picture as below showing

Figure 1-1: FSC-BT3131 Picture

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2. General Specification

Table 2.1: General Specifications

Categories	Features	Implementation
Wireless Specification	Chip	TI CC2340R5
	Bluetooth Version	Bluetooth low energy (BLE) 5.3 Specifications
	Frequency	2.402 - 2.480 GHz
	Transmit Power	+7 dBm (Maximum)
	Receive Sensitivity	-100 dBm (Typical)
	Raw Data Rates (Air)	2 Mbps(Bluetooth 5.3)
Host Interface and Peripherals	UART Interface	TX, RX, CTS, RTS General Purpose I/O Baudrate up to 3Mbps
	I2C Interface	1 (configurable from GPIO total). Up to 400 kbps
	SPI Interface	Primary Mode:SPI clock frequency 12MHz max （1.71 < VDDS < 3.8） Secondary Mode:SPI clock frequency 8MHz max （2.7 < VDDS < 3.8） SCK Duty Cycle 50_{TYP} %
Profiles	Class Bluetooth	No Support
	Bluetooth Low Energy	GATT Client & Peripheral - Any Custom Services BT 5.3 Specifications MFI Support
Maximum Connections	Classic Bluetooth	No Support
	Bluetooth Low Energy	1Clients(TBD)
FW upgrade		Over the Air Xds
Supply Voltage	Supply	1.71V ~ 3.8V
Power Consumption		Max Peak Current(TX Power @ +7dBm): < 11.0 mA Max Peak Current(RX):5.3mA Standby Doze (Wait event) :< 0.7uA (TBD) Deep Sleep < 0.7uA(RTC Running and RAM/CPU Retention) (TBD)
Physical	Dimensions	15.2mm X 25.2mm X 2.4mm, Pad Pitch 1.27mm
Environmental	Operating	-40°C to +125°C
	Storage	-40°C to +125°C
Miscellaneous	Lead Free	Lead-free and RoHS compliant
	Warranty	One Year
Humidity		10% ~ 90% non-condensing
MSL grade:		MSL 3
ESD grade:	Human Body Model	All pins: ±1000V
	Charged device model	RF pins/ Non-RF pins: ±250V

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3. HARDWARE SPECIFICATION

3.1 Block Diagram and PIN Diagram

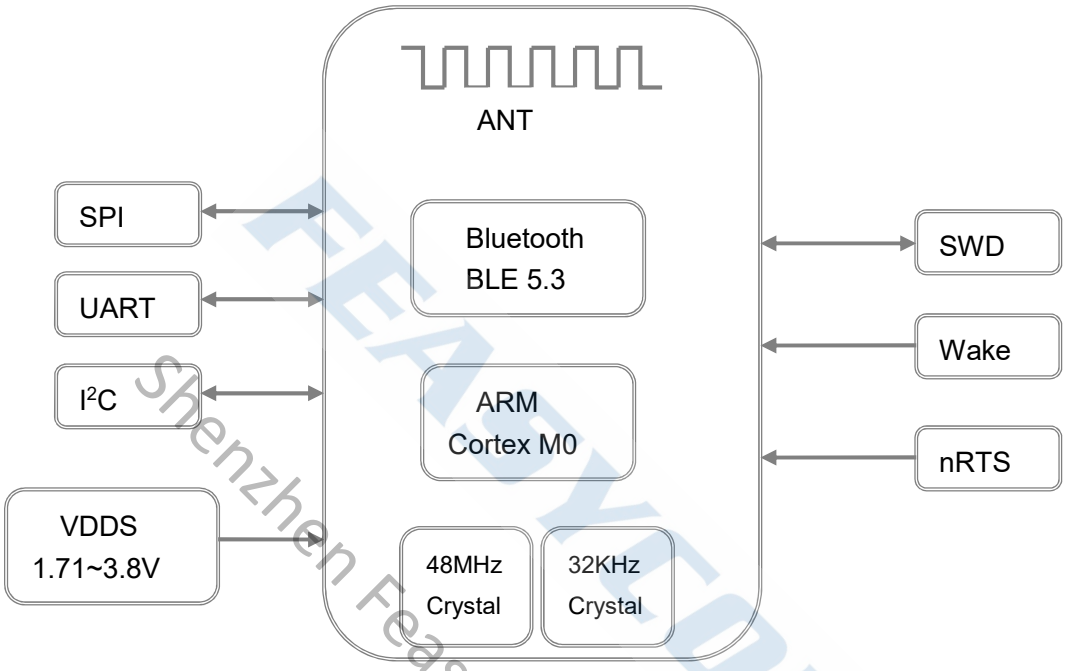

Figure 3-1: FSC-BT3131 Block Diagram

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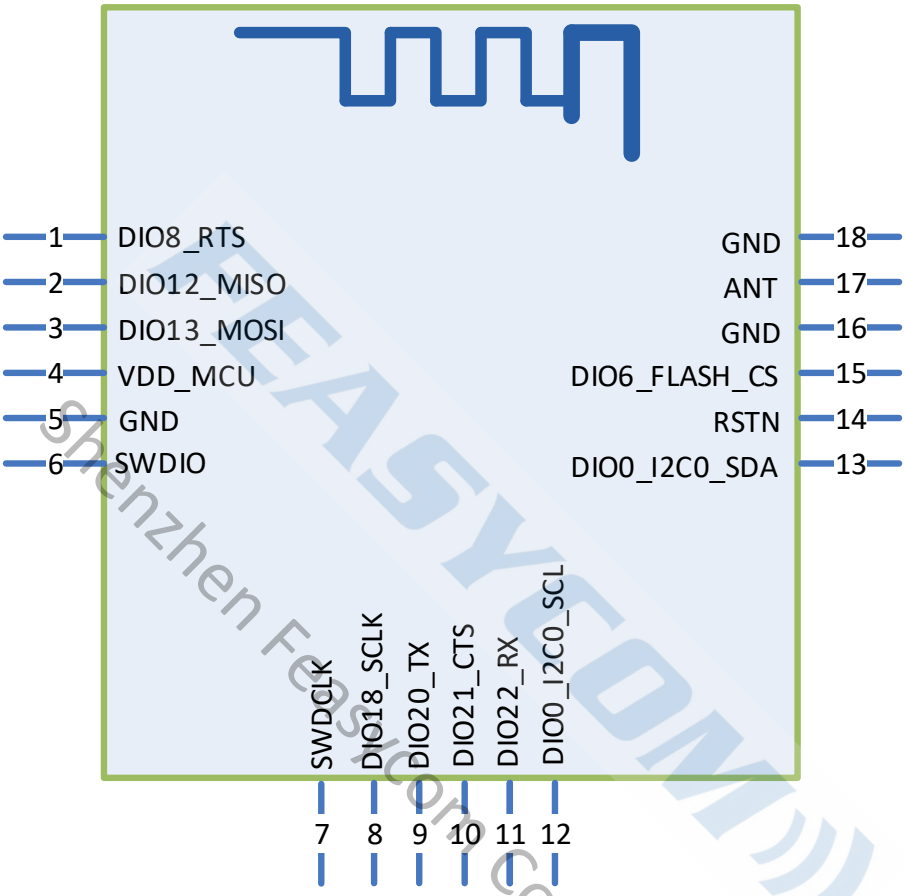

Figure 3-2: FSC-BT3131 PIN Diagram (Top View)

3.2 PIN Definition Descriptions

Table 3.2.1: Pin definition

Pin	Pin Name	Type	Pin Descriptions	Notes
1	DIO8_RTS	I/O	Programmable input/output line Alternative Function: UART request to send active low	Note 1
2	DIO12_MISO	I/O	Programmable input/output line *** The I/O port for reuse.**	Note 4
3	DIO13_MOSI	I/O	Programmable input/output line *** The I/O port for reuse.**	Note 4
4	VDD	Vdd	Power supply voltage 1.8V ~ 3.8V	Power
5	GND	Vss	Power Ground	GND
6	SWDIO	I/O	Debugging through the DATA line(Default)	Note 1

7	SWDCLK	I/O	Debugging through the CLK line(Default)	Note 1
8	DIO18_SCLK	I/O	Programmable input/output line *** The I/O port for reuse.**	Note 4
9	DIO20_TX	O	UART data output	Note 1
10	DIO21_CTS	I/O	Programmable input/output line Alternative Function: UART clear to send active low	Note 1
11	DIO22_RX	I	UART data input	Note 1
12	DIO24_I2C0_SCL	I/O	Programmable input/output line Alternative Function: I2C CLK line (Default)	Note 1,3
13	DIO0_I2C0_SDA	I/O	Programmable input/output line Alternative Function: I2C DATA line (Default)	Note 1,3
14	RSTN	I	External reset input: Active LOW, with an inter an internal pull-up. Set this pin low reset to initial state.	
15	DIO6_FLASH_CS	I/O	Programmable input/output line *** The I/O port for reuse.**	Note 4
16	GND	Vss	Power Ground	GND
17	ANT	RF	Antenna	
18	GND	Vss	Power Ground	GND

Table 3.2.2: Module Pin Notes

Note 1	For customized module, this pin can be work as I/O Interface.
Note 2	BT Status(Default)--Disconnected: Low Level; Connected: High Level.
Note 3	I2C Serial Clock and Data. It is essential to remember that pull-up resistors on both SCL and SDA lines are not provided in the module and MUST be provided external to the module.
Note 4	This I / O port is shared with the internal SPI Flash chip. We do not recommend using this pin, floating processing. This pin is only available when the module is not equipped with air-upgrade function.

4. PHYSICAL INTERFACE

4.1 Power Supply

The transient response of the regulator is important. If the power rails of the module are supplied from an external voltage source, the transient response of any regulator used should be 20μs or less. It is essential that the power rail recovers quickly.

4.2 Reset

The module may be reset from several sources: Power-on Reset (POR), Low level on the nRESET Pin (nRST), Watchdog time-out reset (WDT), Low voltage reset (LVR) or Software Reset(SYSRESETREQ, CPU Reset, CHIPRST).

The RESET pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. A reset will be performed between 1.5 and 4.0ms following RESET being active. It is recommended that RESET be applied for a period greater than 5ms.

At reset the digital I/O pins are set to inputs for bi-directional pins and outputs are tri-state. The PIOs have weak

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pull-ups.

4.3 RF Interface

For This Module, the default mode for antenna is internal ,it also has the interface for external antenna. If you need to use an external antenna, by modifying the module on the 0R resistance to block out the on-board antenna; Or contact Feasycom for modification.

The user can connect a 50 ohm antenna directly to the RF port.

- 2402–2480 MHz Bluetooth 5.3 ; 125 Kbps to 2 Mbps over the air data rate.
- TX output power of +7dBm.
- Receiver to achieve maximum sensitivity -100dBm @ 125 Kbps BLE(BER = 10^{-3}).

4.4 Serial Interfaces

4.4.1 UART

FSC-BT3131 provides one channels of Universal Asynchronous Receiver/Transmitters (UART) (Full-duplex asynchronous communications). The UART Controller performs a serial-to-parallel conversion on data received from the peripheral and a parallel-to-serial conversion on data transmitted from the CPU. Each UART Controller channel supports ten types of interrupts.

This is a standard UART interface for communicating with other serial devices. The UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

When the module is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators.

This module output is at 3.3V CMOS logic levels (tracks VCC). Level conversion must be added to interface with an RS-232 level compliant interface.

Some serial implementations link CTS and RTS to remove the need for handshaking. We do not recommend linking CTS and RTS except for testing and prototyping. If these pins are linked and the host sends data when the FSC-BT617deasserts its RTS signal, there is significant risk that internal receive buffers will overflow, which could lead to an internal processor crash. This drops the connection and may require a power cycle to reset the module. We recommend that you adhere to the correct CTS/RTS handshaking protocol for proper operation.

When connecting the module to a host, please make sure to follow .

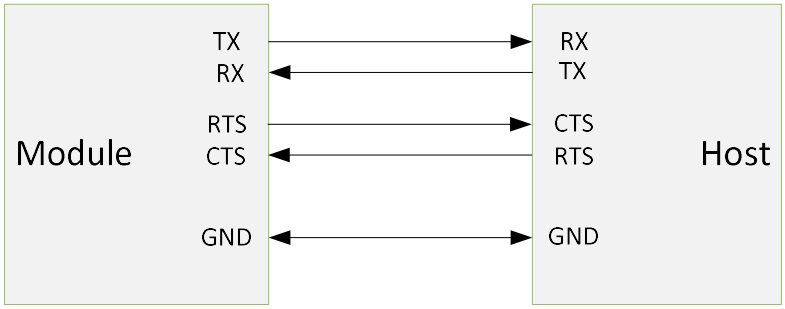

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Figure 4-4: UART Connection

4.4.2 I2C Interface

- Up to two I²C bus interfaces can support both master and slave mode with a frequency up to 400KHZ.
- Provide arbitration function, optional PEC(packet error checking) generation and checking.
- Supports 7 –bit and 10 –bit addressing mode and general call addressing mode.

The I²C interface is an internal circuit allowing communication with an external I²C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I²C module provides two data transfer rates: 100 kHz of standard mode or 400kHz of the fast mode. The I²C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I²C bus at the same time. A CRC-8 calculator is also provided in I²C interface to perform packet error checking for I²C data.

4.5 SPI Interface

The SPI module supports both SPI controller and peripheral up to 12 MHz with configurable phase and polarity.

5. ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

Absolute maximum ratings for supply voltage and voltages on digital and analogue pins of the module are listed below. Exceeding these values causes permanent damage.

The average PIO pin output current is defined as the average current value flowing through any one of the corresponding pins for a 100mS period. The total average PIO pin output current is defined as the average current value flowing through all of the corresponding pins for a 100mS period. The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

Table 5.1: Absolute Maximum Rating

Parameter	Min	Max	Unit
VDDS - DC Power Supply	-0.3	+4.1	V
Input RF level		5	dBm
TST - Storage Temperature	-40	+125	°C
IIO - Maximum Current sunk by a I/O pin		8	mA
IIO - Maximum Current sourced by a I/O pin		8	mA

5.2 Recommended Operating Conditions

Table 5.2: Recommended Operating Conditions

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Parameter	Min	Type	Max	Unit
VDDS - DC Power Supply	1.8	3.3	3.8	V
T_A - Operating Temperature	-40	25	+125	°C
I_{IO} - Maximum Current sunk by a I/O pin	2	4	6	mA
I_{IO} - Maximum Current sourced by a I/O pin	2	4	6	mA

5.3 SPI Characteristics

Table 5.3: SPI Characteristics

Symbol	Parameter		Min	Type	Max	Unit
fSCLK 1/tsclk	SPI clock frequency	Primary Mode 1.71 < VDDS < 3.8			12	MHz
		Secondary Mode 2.7 < VDDS < 3.8			8	MHz
		Secondary Mode VDDS < 2.7			7	MHz
DCsck	SCK Duty Cycle		45	50	55	%

5.4 SPI Interface (Controller Mode)

Table 5.4: SPI Interface (Controller Mode)

Symbol	Parameter	Min	Type	Max	Unit
$t_{SCLK\_H/L}$	SCLK High or Low time		$t_{SPI}/2$		ns
$t_{CS.LEAD}$	CS lead-time, CS active to clock	1			SCLK
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive	1			SCLK
$t_{CS.ACC}$	CS access time, CS active to PICO data out			1	SCLK
$t_{CS.DIS}$	CS disable time, CS inactive to PICO high inpedance			1	SCLK
$t_{VALID.CO}$	PICO output data valid time(1) SCLK edge to PICO valid,CL = 20 pF			13	ns
$t_{HD.CO}$	PICO output data hold time(2) CL = 20 pF	0			ns

(1) Specifies the time to drive the next valid data to the output after the output changing SCLK clock edge
(2) Specifies how long data on the output is valid after the output changing SCLK clock edge

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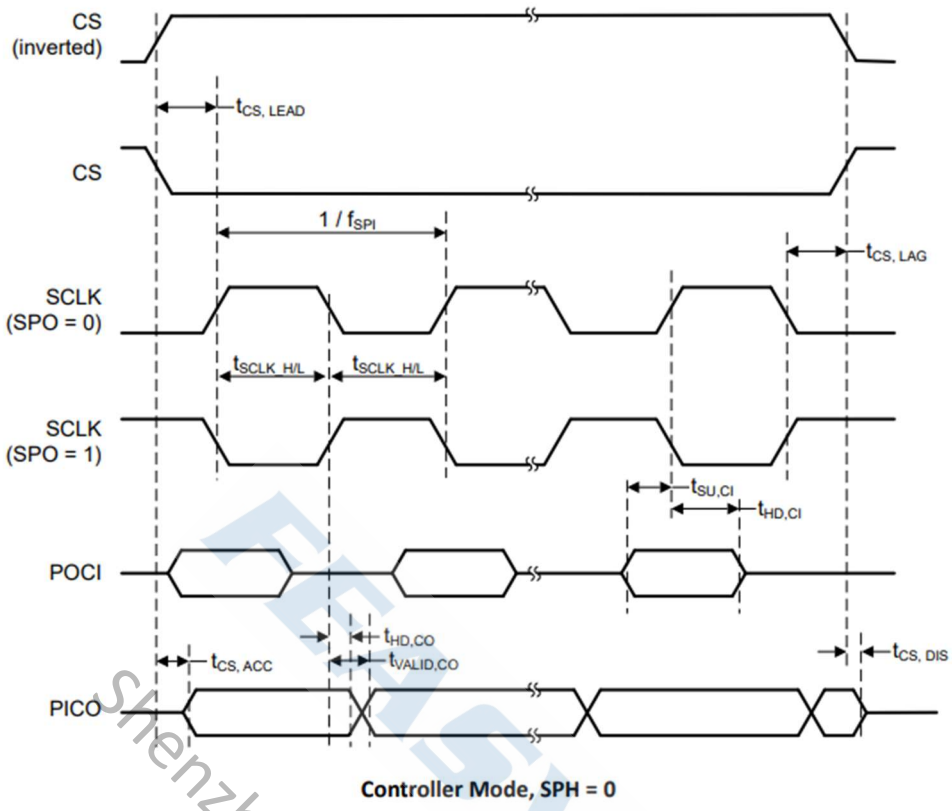

Figure 5-4-1:SPI Timing Diagram - Controller Mode, SPH = 0

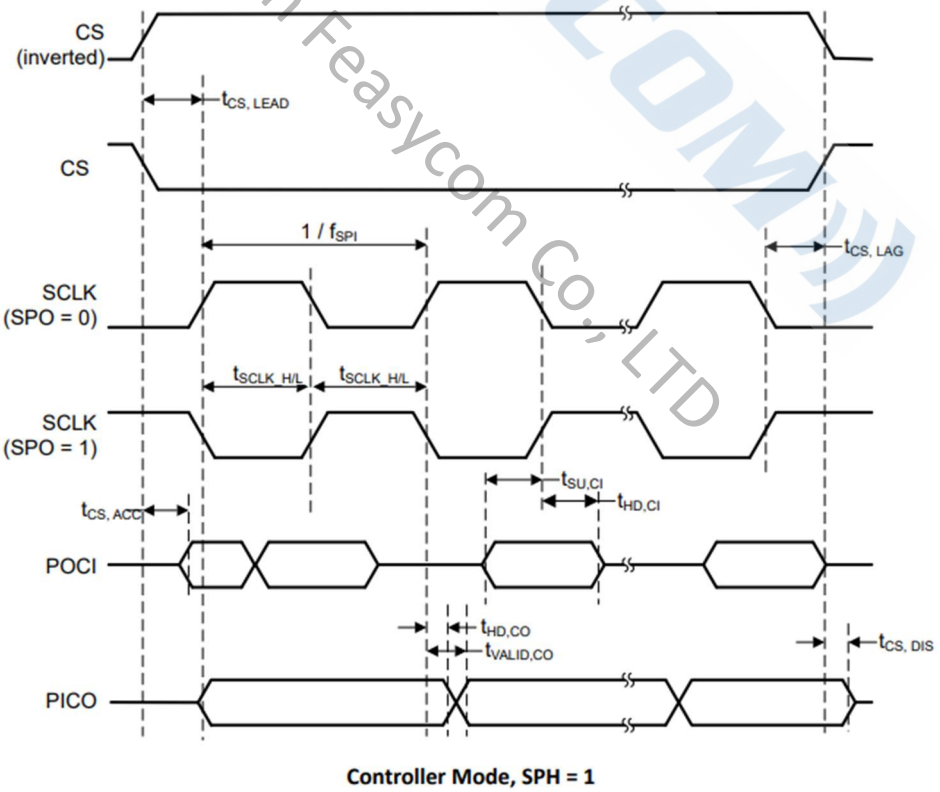

Figure 5-4-2: SPI Timing Diagram - Controller Mode, SPH = 1

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5.5 SPI Interface (Peripheral Mode)

Table 5.5: Synchronous Serial Interface (SSI) (Tc = 25°C, VDD = 3.0 V, unless otherwise noted.)

Symbol	Parameter	Min	Type	Max	Unit
$t_{CS,\ LAG}$	CS lead-time, CS active to clock	1			SCLK
$t_{CS,\ LAG}$	CS lag time, Last clock to CS inactive	1			SCLK
$t_{CS,\ Acc}$	CS access time, CS active to POCI data out VDDS = 3.3V			56	ns
$t_{CS,\ Acc}$	CS access time, CS active to POCI data out VDDS = 1.8V			70	ns
$t_{CS,\ DIS}$	CS disable time, CS inactive to POCI high impedance VDDS = 3.3V			56	ns
$t_{CS,\ DIS}$	CS disable time, CS inactive to POCI high impedance VDDS = 1.8V			70	ns
$t_{SU,\ PI}$	PICO input data setup time	30			ns
$t_{HD,\ PI}$	PICO input data hold time	0			ns
$t_{VALID,\ PO}$	POCI output data valid time(1) SCLK edge to POCI valid,CL = 20 pF, 3.3V (4)			50	ns
$t_{VALID,\ PO}$	POCI output data valid time(1) SCLK edge to POCI valid,CL = 20 pF, 1.8V (4)			65	ns
$t_{HD,\ PO}$	POCI output data hold time(2) CL = 20 pF	0			ns

(1) Specifies the time to drive the next valid data to the output after the output changing SCLK clock edge
(2) Specifies how long data on the output is valid after the output changing SCLK clock edge

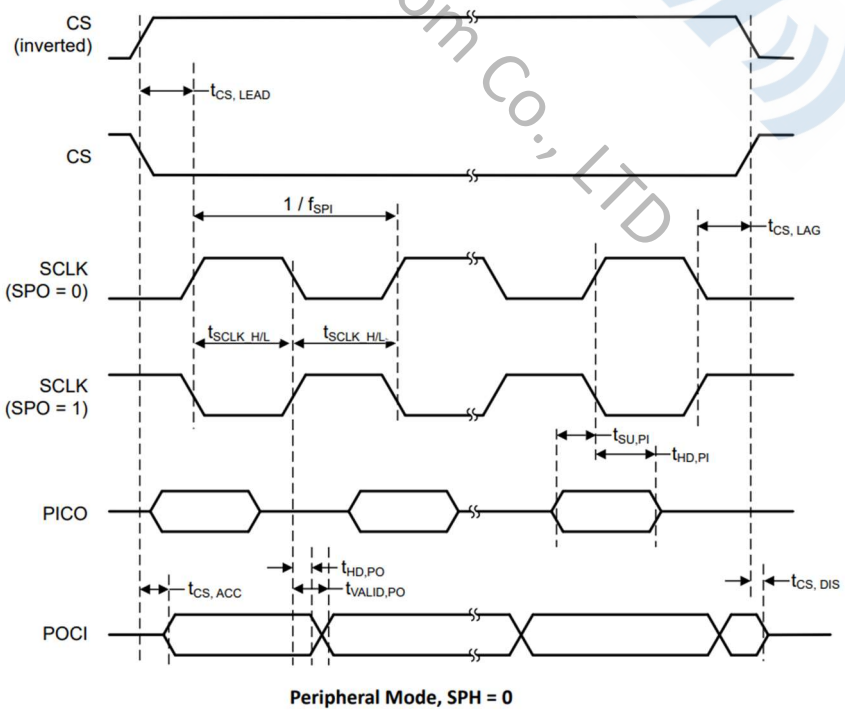

Figure 5-5-1: SPI Timing Diagram - Peripheral Mode, SPH =0

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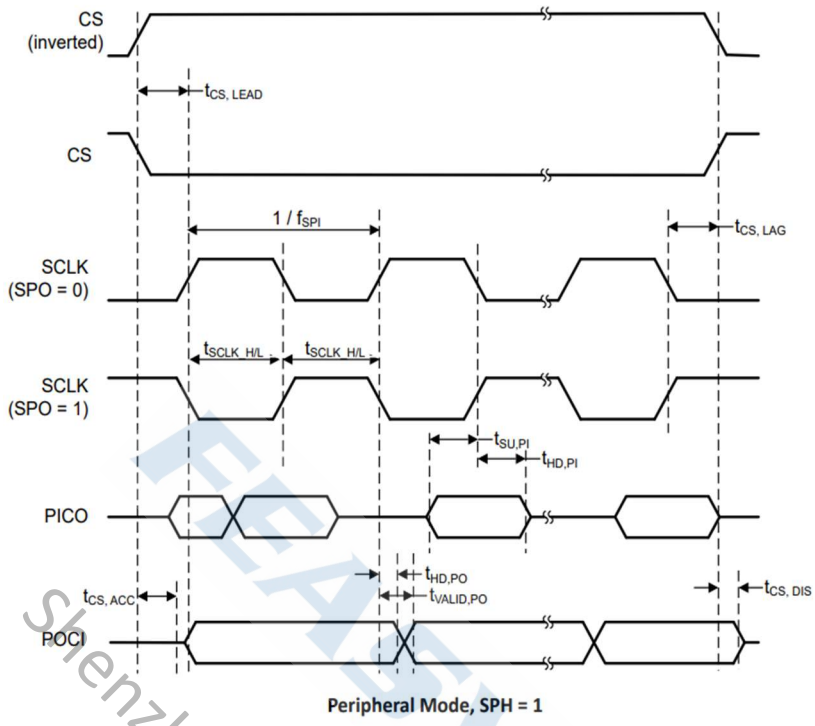

Figure 5-5-2: SPI Timing Diagram - Peripheral Mode, SPH = 1

5.6 Power consumptions-Power Modes

Table 5.6: Power consumptions（with Tc = 25 °C, VDDS = 3.0 V, DCDC enabled, GLDO disabled, unless otherwise noted.）

Parameter		Test Conditions	Type	Unit
Icore	Active	MCU running CoreMark from Flash at 48 MHz	2.6	mA
Icore	Idle	Supply Systems and RAM powered, flash disabled, DMA disabled	1100	uA
Icore	Standby	RTC running, 36kB RAM retention LFOSC, DCDC recharge current setting (ipeak = 1)	0.71	
Core Current consumption with GLDO				
Icore	Active	MCU running CoreMark from Flash at 48 MHz	4.1	mA
Icore	Idle	Supply Systems and RAM powered, flash enabled, DMA disabled	1490	uA
Icore	Standby	RTC running, 36kB RAM retention LFOSC, default GLDO recharge current setting	1.1	uA
Reset, Shutdown Current Consumption				
Icore	Reset	Reset. RSTN pin asserted or VDDS below power-on-reset threshold	150	nA
Icore	Shutdown	Shutdown measured in steady state. No clocks running, no retention, IO wakeup enabled	150	nA
Peripheral Current Consumption				
Iperi	RF	Delta current, clock enabled, RF subsystem idle	40	uA
Iperi	I2C	Delta current with clock enabled, module is idle	10.6	uA
Iperi	SP	Delta current with clock enabled, module is idle	3.4	uA
Iperi	UART	Delta current with clock enabled, module is idle	24.5	uA

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5.7 Power consumptions-Radio Modes

Table 5.7: Power consumptions（with Tc = 25 °C, VDDS = 3.0 V, DCDC enabled, GLDO disabled, unless otherwise noted.）

Parameter		Test Conditions	Type	Unit
I_{RX}	Radio receive current	2440 MHz, 1 Mbps, GFSK, system bus off (1)	5.3	mA
I_{RX}	Radio receive current	2440 MHz, 1 Mbps, GFSK, DCDC OFF, system bus off (1)	9	mA
I_{Tx}	Radio transmit current	-8 dBm output power setting 2440 MHz system bus off (1)	4.0	mA
I_{Tx}	Radio transmit current	0 dBm output power setting 2440 MHz system bus off (1)	5.1	mA
I_{Tx}	Radio transmit current	0 dBm output power setting 2440 MHz DCDC OFF, system bus off (1)	8.8	mA
I_{Tx}	Radio transmit current	+4 dBm output power setting 2440 MHz system bus off (1)	7.7	mA
I_{Tx}	Radio transmit current	+6 dBm output power setting 2440 MHz system bus off (1)	8.9	mA
I_{Tx}	Radio transmit current	+7 dBm output power setting 2440 MHz system bus off (1)	10.7	mA
I_{Tx}	Radio transmit current	+7 dBm output power setting 2440 MHz DCDC OFF, system bus off (1)	19	mA

(1) System bus off refers to device idle mode, DMA disabled, flash disabled

6. MSL &ESD

Table 6.0: MSL and ESD

Parameter	Test Conditions		Value
MSL grade:	MSL 3(1)		
ESD grade:	Human body model (HBM), per ANSI/ESDA/JEDEC JS001(2)	All pins	±1000V
	Charged device model (CDM), per JESD22-C101(3)	RF pins	±250V
		Non-RF pins	±250V

(1)The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7. RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccate (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the Picture below and follow instructions specified by IPC/JEDEC J-STD-033.

Note: The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the Picture below, the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccate and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60%RH.

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Table 7.0: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated@ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Feasycom surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

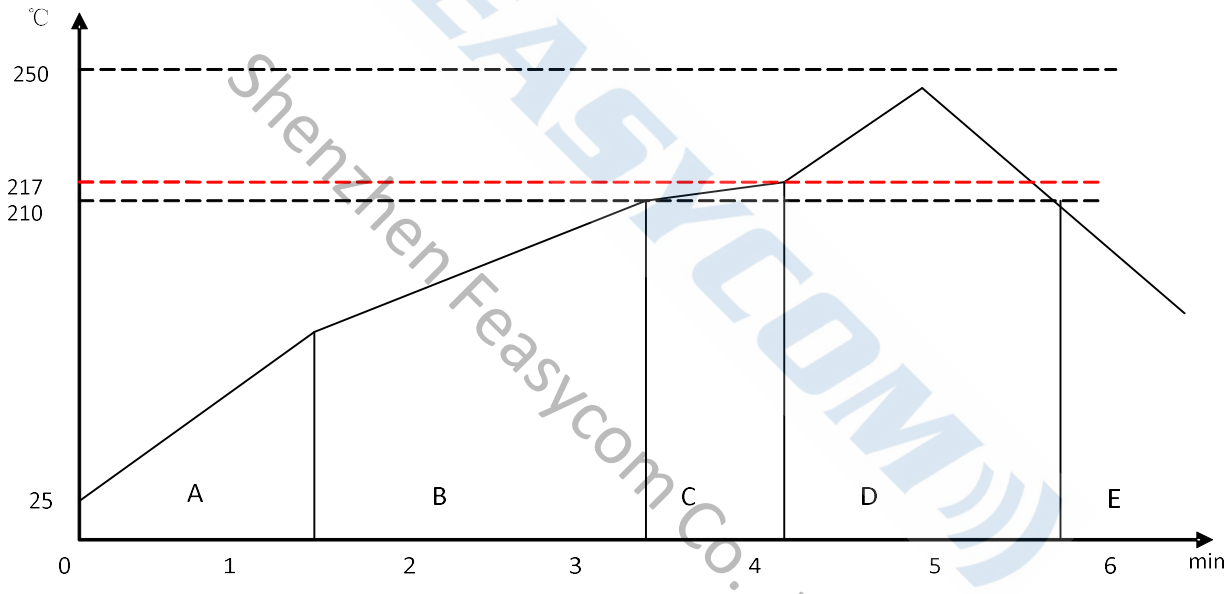

Figure 7-1: Typical Lead-free Re-flow

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

Equilibrium Zone 2 (C) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The

recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

8. MECHANICAL DETAILS

8.1 Mechanical Details

- Dimension: 15.2mm(W) x 25.2mm(L) x 2.4 mm(H) Tolerance: ±0.1mm
- Module size: 15.2mm X 25.2mm Tolerance: ±0.2mm
- Pad size: 1.8mmX0.8mm Tolerance: ±0.1mm
- Pad pitch: 1.27mm Tolerance: ±0.1mm

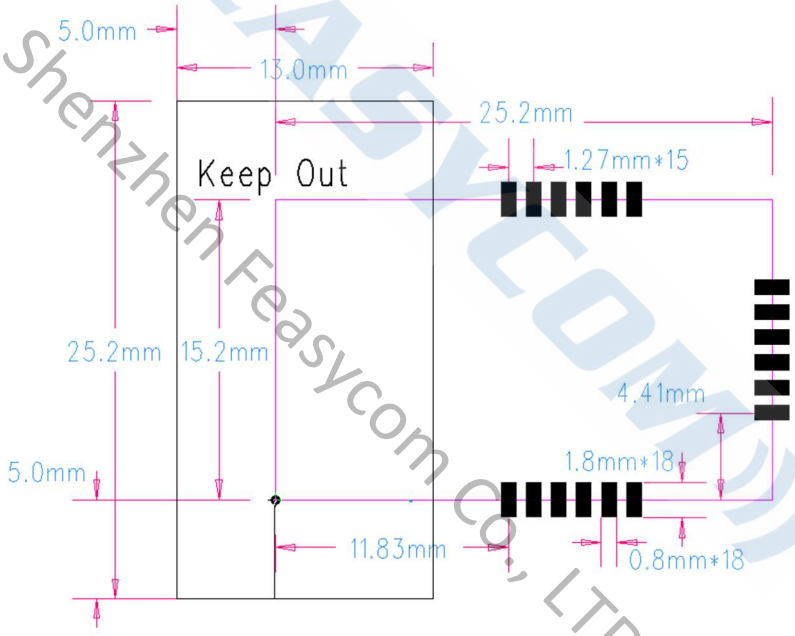

Figure 8-1: FSC-BT3131 Recommended Footprint

9. HARDWARE INTEGRATION SUGGESTIONS

9.1 Soldering Recommendations

FSC-BT617 is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

9.2 Layout Guidelines(Internal Antenna)

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.

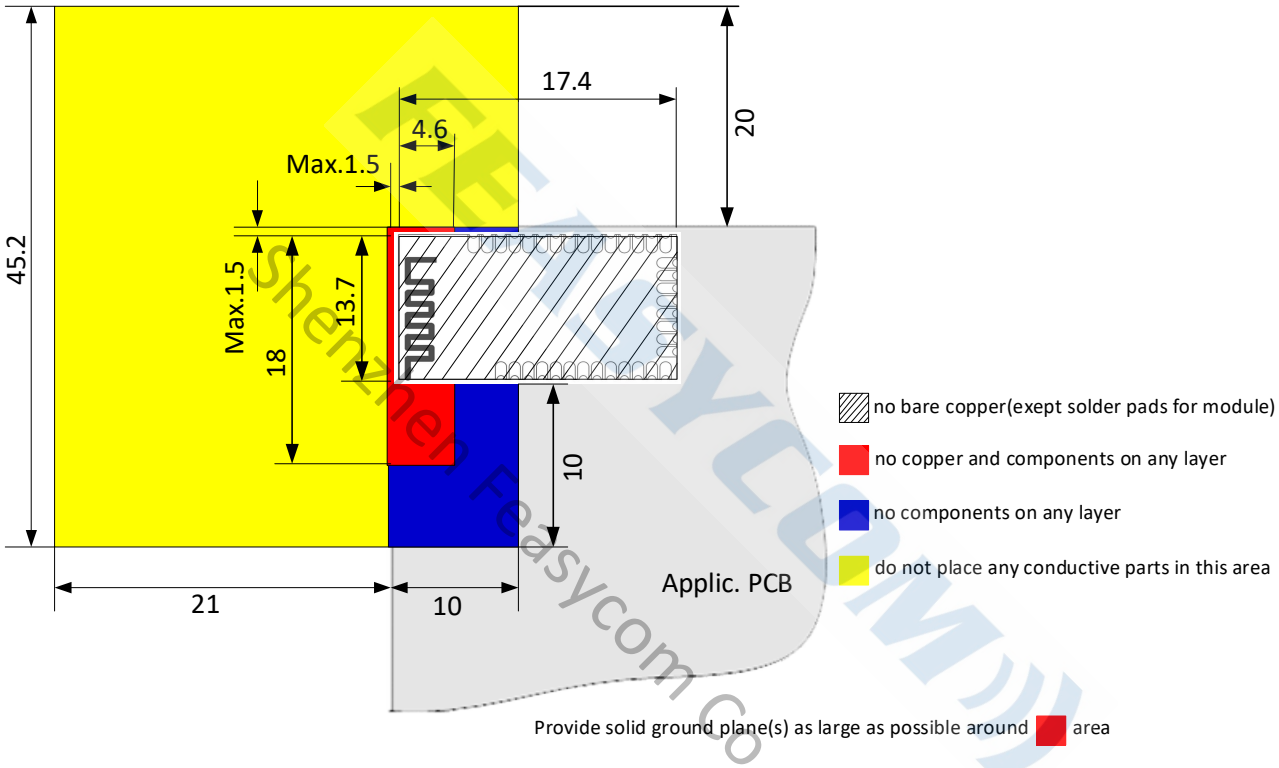

Figure 9-2: FSC-BT3131 Restricted Area

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

9.3 Layout Guidelines(External Antenna)

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible

to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in picture below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

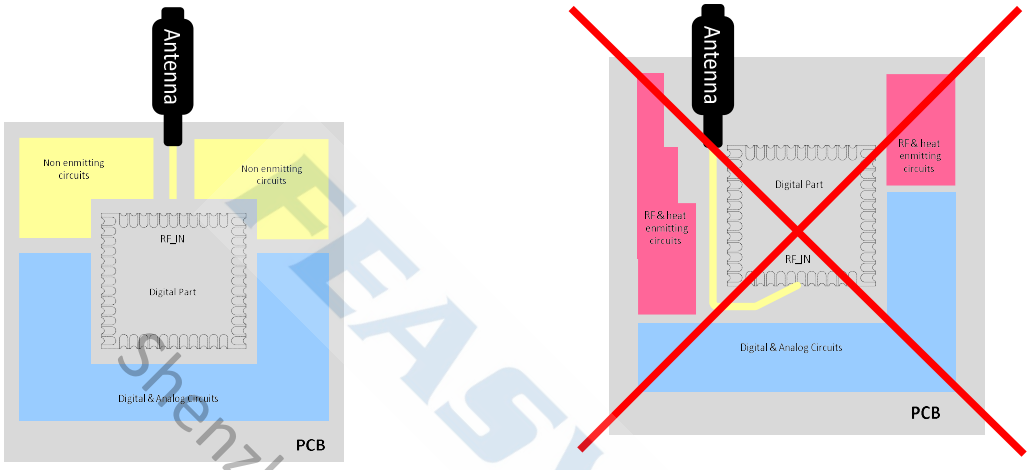

Figure 9-3: Placement the Module on a System Board

9.4 Antenna Connection and Grounding Plane Design

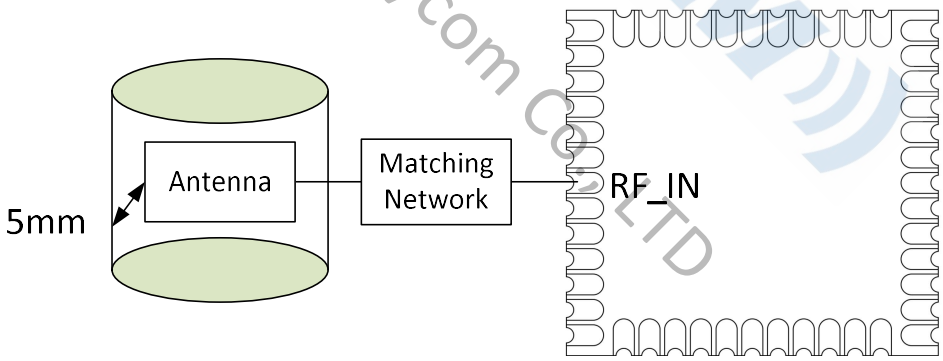

Figure 9-4-1: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

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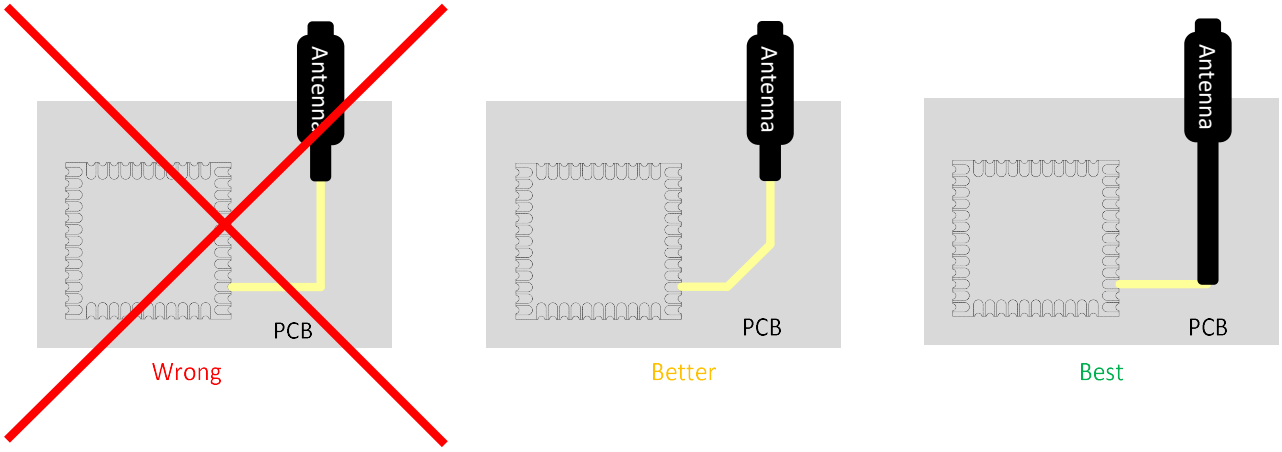

Figure 9-4-2: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.
-

10. PRODUCT PACKAGING INFORMATION

10.1 DefaultPacking

a, Tray vacuum

b, Tray Dimension: 180mm * 195mm

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Figure 10-1: Tray vacuum

10.2 Packing box(Optional)

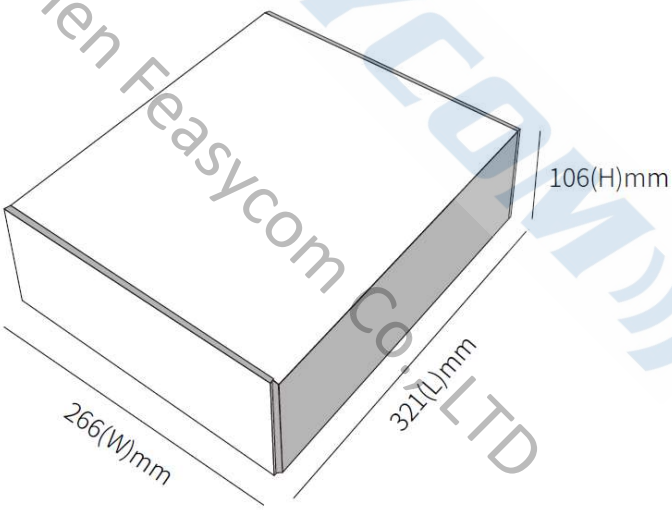

Figure 10-2: Packing Box

* If require any other packing, must be confirmed with customer

* Package: 1000PCS Per Carton (Min Carton Package)

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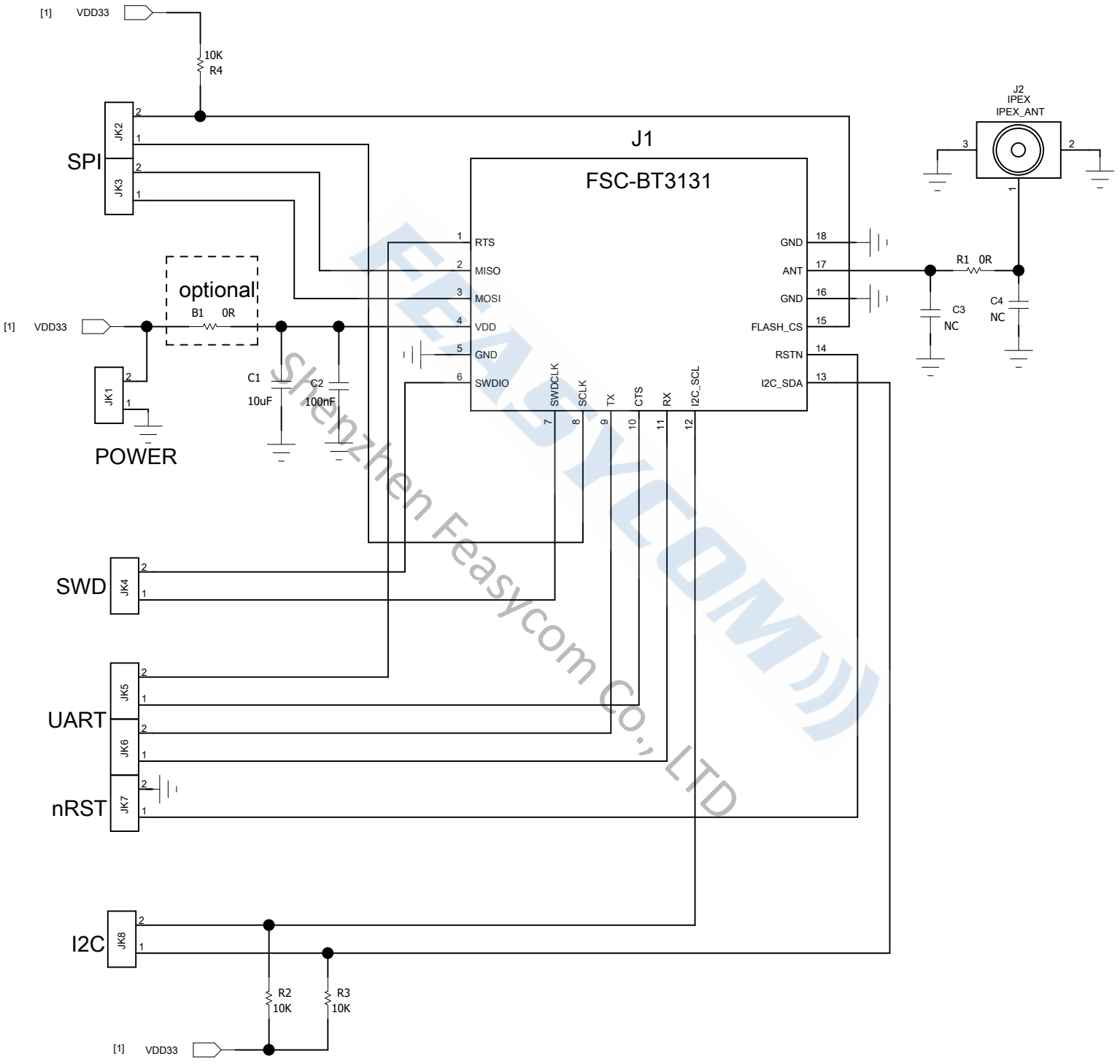
11.APPLICATION SCHEMATIC:



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