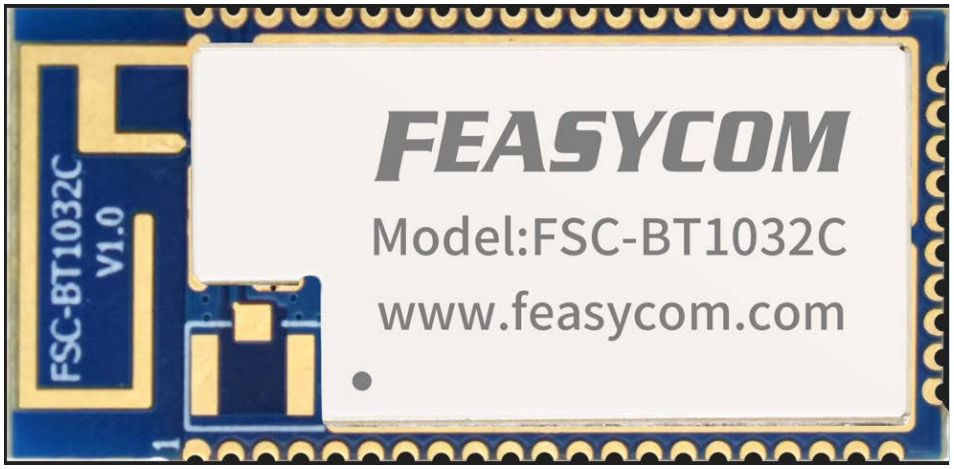

FSC-BT1032C

DATASHEET V1.01

1 INTRODUCTION

Overview

FSC-BT1032C it is a Bluetooth dual-mode module series. It supports a Bluetooth Low Energy and compliant system for audio and data communication.

FSC-BT1032C integrates application processor with embedded flash memory, a high-performance stereo codec, a power management subsystem, I^2S, LED drivers and ADC I/O.

By default, FSC-BT1032C module is equipped with powerful and easy-to-use Feasycom firmware. It's easy to use and completely encapsulated. Feasycom firmware enables users to access Bluetooth functionality with simple ASCII commands delivered to the module over serial interface - it's just like a Bluetooth modem.

Therefore, FSC-BT1032C provides an ideal solution for developers who want to integrate Bluetooth wireless technology into their design.

Features

- Bluetooth® v5.2 specification
- 32-bit MCU at up to 120 MHz
- Digital interfaces: I^2S/PCM
- Low power consumption: A2DP 2.8mA , Shutdown: 0.8 μA
- 2x audio ADC/DAC
- Up to 6x 32-bit PWM
- UART for debugging and downloading

Application

- TWS
- Wireless Audio

2 General Specification

Table 2-1：General Specifications

Categories	Features	Implementation
Bluetooth		
	Chip	FSC2092
	Bluetooth Standard	Bluetooth v5.2
	Frequency Band	2402MHz~2480MHz
	Transmit Power	Basic Rate :+8 dBm (Typ VBAT=3.3V)
	Receiver	Basic rate: -95dBm (Typ VBAT=3.3V)
	Interface	UART/PCM/ Analog audio
Size		13mm × 26.9 mm × 2.2mm
Operating temperature		-20°C ~+85°C,
Storage temperature		-40°C ~+85°C
Supply Voltage		3.0V~4.2V
Miscellaneous	Lead Free Warranty	Lead-free and RoHS compliant One Year
Humidity		10% ~ 90% non-condensing
MSL grade:		MSL 3
ESD grade:		Human Body Model: Pass ±2000 V, all pins Charge device model: Pass ±500 V, all pins

3 HARDWARE SPECIFICATION

3.1 Block Diagram and PIN Diagram

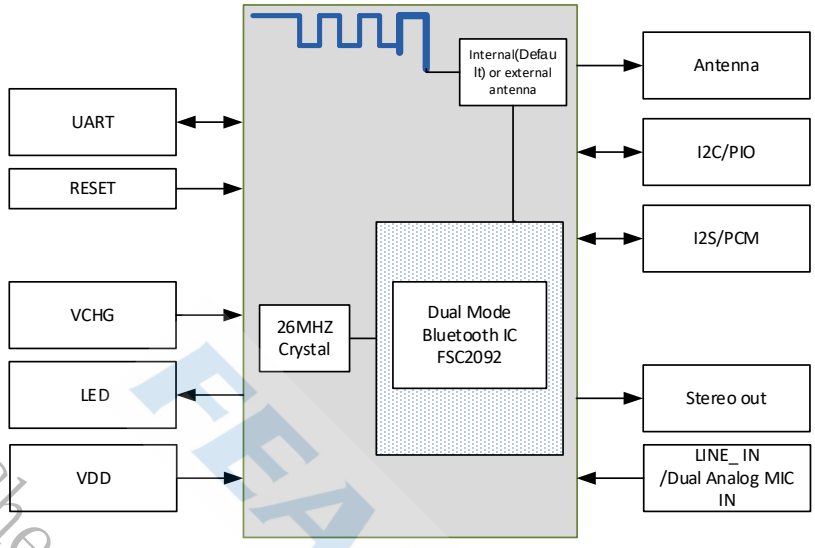

Figure 3-1:Block Diagram

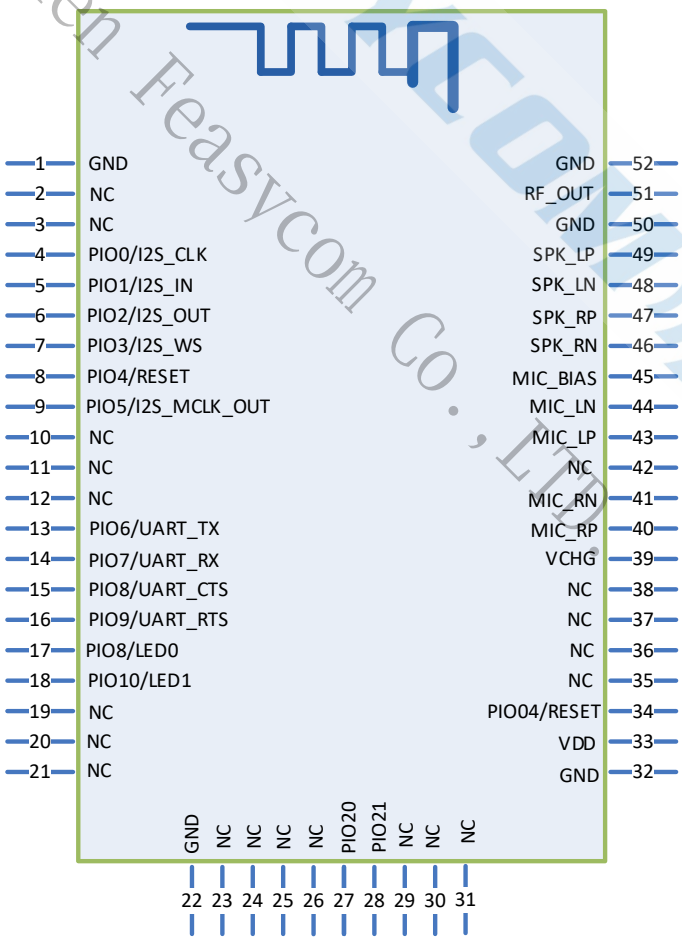

Figure 3-2:FSC-BT1032C PIN Diagram(Top View)

3.2 PIN Definition Descriptions

Table 3-2：Pin definition

Pin	Pin Name	Type	Pin Descriptions	Notes
1	GND	Vss	Power Ground	
2	NC			
3	NC			
4	PIO0/I²S_CLK	I/O	Programmable I/O line 0. Alternative function: I²S _CLK	
5	PIO1/I²S _IN	I/O	Programmable I/O line 1. Alternative function: I²S _DIN	
6	PIO2/I²S _OUT	I/O	Programmable I/O line 2. Alternative function: I²S _DOUT	
7	PIO3/I²S _WS	I/O	Programmable I/O line 3. Alternative function: I²S _WS	
8	PIO4/RESET	I/O	Programmable I/O line 4. Alternative function:RESET	
9	PIO5/I²S _MCLK_OUT	I/O	Programmable I/O line 5. Alternative function: MCLK_OUT	
10	NC			
11	NC			
12	NC			
13	PIO6/UART_TX	I/O	Programmable I/O line 6. Alternative function: UART_TX	
14	PIO7/UART_RX	I/O	Programmable I/O line 7. Alternative function: UART_RX	
15	PIO8/ UART_CTS	I/O	Programmable I/O line 8 Alternative function: UART_ CTS	
16	PIO9/ UART_RTS	I/O	Programmable I/O line 9 Alternative function: UART_ RTS	
17	PIO8/LED0	A,I/O	Programmable I/O line 8 Alternative function: LED0	
18	PIO10/LED1	A,I/O	Programmable I/O line 10 Alternative function: LED1	
19	NC			
20	NC			

21	NC		
22	GND	Vss	Power Ground
23	NC		
24	NC		
25	NC		
26	NC		
27	PIO20	I/O	Programmable I/O line 20.
28	PIO21	I/O	Programmable I/O line 21.
29	NC		
30	NC		
31	NC		
32	GND	Vss	Power Ground
33	VDD	Vdd	SYS Power(3.0~4.2V)
34	PIO4/RESET	I	
35	NC		
36	NC		
37	NC		
38	NC		
39	VCHG	Vdd	Charger input to Bypass regulator.（USB VBUS 4.75~5.25V）
40	MIC_RP	A	Microphone differential 2 input, positive. Alternative function: Differential audio line input right, positive
41	MIC_RN	A	Microphone differential 2 input, negative. Alternative function: Differential audio line input right, negative
42	NC		
43	MIC_LP	A	Microphone differential 1 input, positive. Alternative function: Differential audio line input left, positive
44	MIC_LN	A	Microphone differential 1 input, negative. Alternative function: Differential audio line input left, negative
45	MIC_BIAS	Vdd	Mic bias output.
46	SPK_RN	A	Differential line output, negative
47	SPK_RP	A	Differential line output, positive
48	SPK_LN	A	Differential line output, negative
49	SPK_LP	A	Differential line output, positive

50	GND	Vss	Power Ground
51	RF_OUT	RF	Bluetooth transmit/receive.
52	GND	Vss	Power Ground

4 PHYSICAL INTERFACE

4.1 UART Interface

FSC-BT1032C includes two Universal Asynchronous Receiver/Transmitter (UART) interfaces, UART1 and UART2, which offer full-duplex, asynchronous serial communication at a baud rate up to 3.25 Mbps. They support 5/6/7/8 bits data, and even, odd or none parity check. The stop bit can be either 1 bit or 2 bits.

Table 4-1： Possible UART Settings

Parameter	Possible Values
Baudrate	Minimum 1200 baud (≤0%Error) Standard 115200bps(≤0.08%Error) Maximum 3.25 Mbps(≤0%Error)
Flow control	Supports Automatic Flow Control (CTS and RTS lines)
Parity	None, Odd or Even
Number of stop bits	1
Bits per channel	8

4.2 I²S

FSC-BT1032C integrates a I2S interface. The I2S interface supports both master and slave mode with sample rates from 8 kHz to 384 kHz.

4.3 Analog Peripherals

FSC-BT1032C comes with a rich set of audio peripherals to enhance the Bluetooth listening experience. The chip includes a four-band digital equalizer, two analog-to-digital converters (ADC) and two digital-to-analog converters (DAC)

4.3.1 Audio ADC and DAC

FSC-BT1032C contains two high fidelity ADCs with sample rates of 8 kHz, 16 kHz, 44.1 kHz, or 48 kHz. The chip also integrates high fidelity stereo DACs with sample rates of 8 kHz, 16 kHz, 44.1 kHz or 48 kHz.

4.3.2 Microphone Input Amplifier and Bias

FSC-1032C contains a fully differential analog microphone input amplifier and a low-noise microphone bias generator. Expensive external components are not needed as the microphone amplifier and active bias circuitry are integrated into the chip, allowing the microphone to interface with passive resistors and capacitors.

The microphone signal can be amplified with gain from 0 to 32 dB with 2 dB step.

4.3.3 Audio Output

FSC-1032C provides high fidelity stereo audio L/R outputs capable of driving 16 Ω speakers with up to 30 pF of load capacitance.

4.3.4 Four-Band Digital Equalizer

A dedicated four-band digital equalizer is implemented prior to digital-to-analog conversion to give users the option of customizing the frequency response of the audio output. The equalizer is implemented in hardware to reduce overall chip power consumption.

4.4 Reset

A reset can be triggered by the following sources: Power-on reset, brown-out reset, watchdog reset, low level on RSTN pin (external reset), software reset, and wakeup from shutdown mode or deep sleep mode.

System power on, digital power on and watchdog reset have the same reset effect one major blocks except always on logic, that any reset will reset the whole chip to initial status. The always on logic has one 32-bit timer and 16-bit retention registers, which can only be reset to initial value by system power on reset.

Wakeup from either shutdown mode or deep sleep mode will power on digital from power down mode, which triggers the whole system reset procedure.

4.5 Standard PIO

FSC-1032C has up to 11 GPIOs. Each can be configured as either input or output. Each GPIO has alternate functions.

All GPIO pins can wake up the internal MCU from deep sleep mode. In deep sleep mode, any level change on the set GPIO will trigger the wakeup procedure.

5 ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

All measurements are referenced at the module pins unless otherwise indicated. All specifications are over process and voltage unless otherwise indicated.

Over operating free-air temperature range (unless otherwise noted)

Table 5-1：Absolute Maximum Rating

Parameter	Min	Type	Max	Unit
VCHG	-0.3		+5.75	V
VDD	-0.4		+4.5	V
Storage temperature (T_{stg})	-40		+85	°C

5.2 Recommended Operating Conditions

Table 5-2：Recommended Operating Conditions

Parameter	Min	Type	Max	Unit
VCHG	4.75	5.0	+5.75	V
VDD	3.0	3.3	+4.2	V
MIC_BIAS	1.8		2.4	V
Operating temperature (T_A)	-20		+85	°C

5.3 RF Characteristic

Table 5-3: RF Characteristics performance at 25°C

Characteristics	Condition	Min	Type	Max	Unit
Frequency range		2400		2527	MHz
Maximum RF transmit power		-	8	-	dBm
RX Sensitivity	GFSK, 0.1% BER, 1 Mbps		-93	-	dBm
	π /4-DQPSK, 0.01% BER, 2 Mbps		-95	-	dBm
	8-DPSK, 0.01% BER, 3 Mbps		TBD	-	dBm
Maximum received signal	0.1% BER	-	0	-	dBm

5.4 Audio Characteristic

Table 5-4：DAC Characteristics performance at 25°C

Characteristics	Condition	Min	Type	Max	Unit
Output	RL=600 Ohm	-	1	-	Vrms
	RL=16 Ohm	-	0.8	-	Vrms
THD	RL=600 Ohm	-	-	-80	dB
	RL=16 Ohm	-	-	-80	dB
SNR	1 kHz sine wave	-	104	-	dB
Sample Rate		8		48	KHz

Table 5-4-1：ADC Characteristics performance at 25°C

Characteristics	Condition	Min	Type	Max	Unit
SNR	1 kHz sine wave	-	100	-	dB
Sample Rate		8	-	48	KHz

6 MSL & ESD

Table 6-1: MSL and ESD

Parameter	Value
MSL grade:	MSL 3
ESD grade	Electrostatic discharge
ESD – Human-body model (HBM) rating, JESD22-A114-F (Total samples from one wafer lot)	Pass ±2000 V, all pins
ESD – Charge-device model (CDM) rating, JESD22-C101-D (Total samples from one wafer lot)	Pass ±400 V, all pins

7 RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccate (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the below and follow instructions specified by IPC/JEDEC J-STD-033.

Note: The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the below , the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccate and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60%RH.

Notice (注意) :

Feasycom module must use Step-Stencil, suggestion using the stencil thickness about 0.16-0.2mm,it could be modify with the product.

Table 7-1: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Feasycom surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

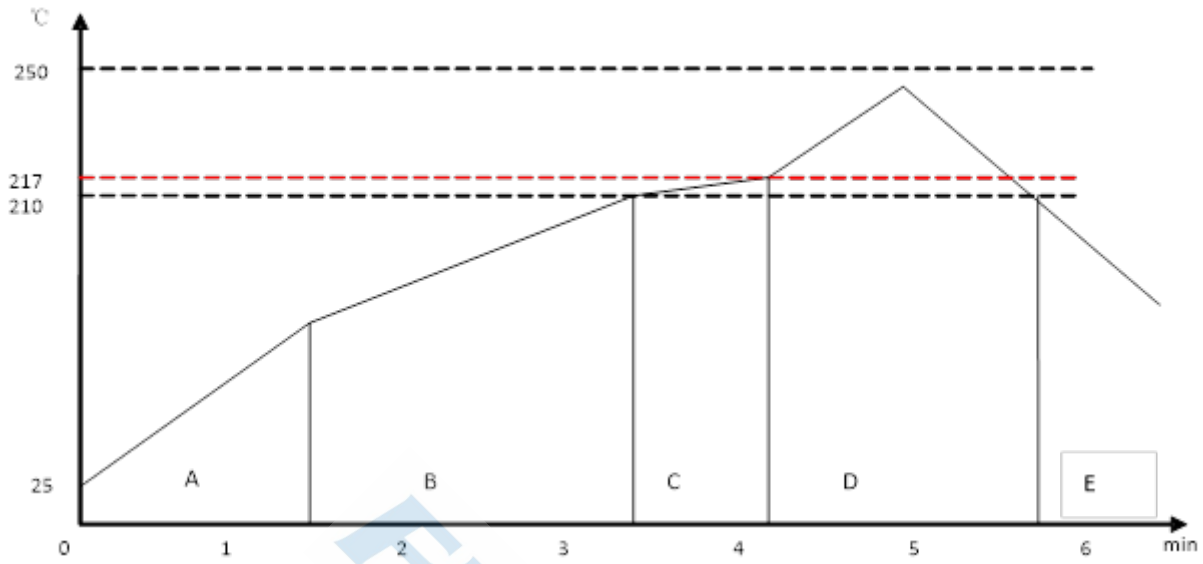

Figure 7-1：Typical Lead-free Re-flow

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

Equilibrium Zone 2 (C) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

8 MECHANICAL DETAILS

8.1 Mechanical Details

- Dimension: 13mm(W) x 26.9mm(L) x 2.2mm(H) Tolerance: ±0.2mm
- Module size: 13mm X 26.9mm Tolerance: ±0.2mm
- Pad size: 1.6mmX0.6mm Tolerance: ±0.2mm
- Pad pitch: 1.0mm Tolerance: ±0.1mm
- **(Residual plate edge error: < 0.5mm)**

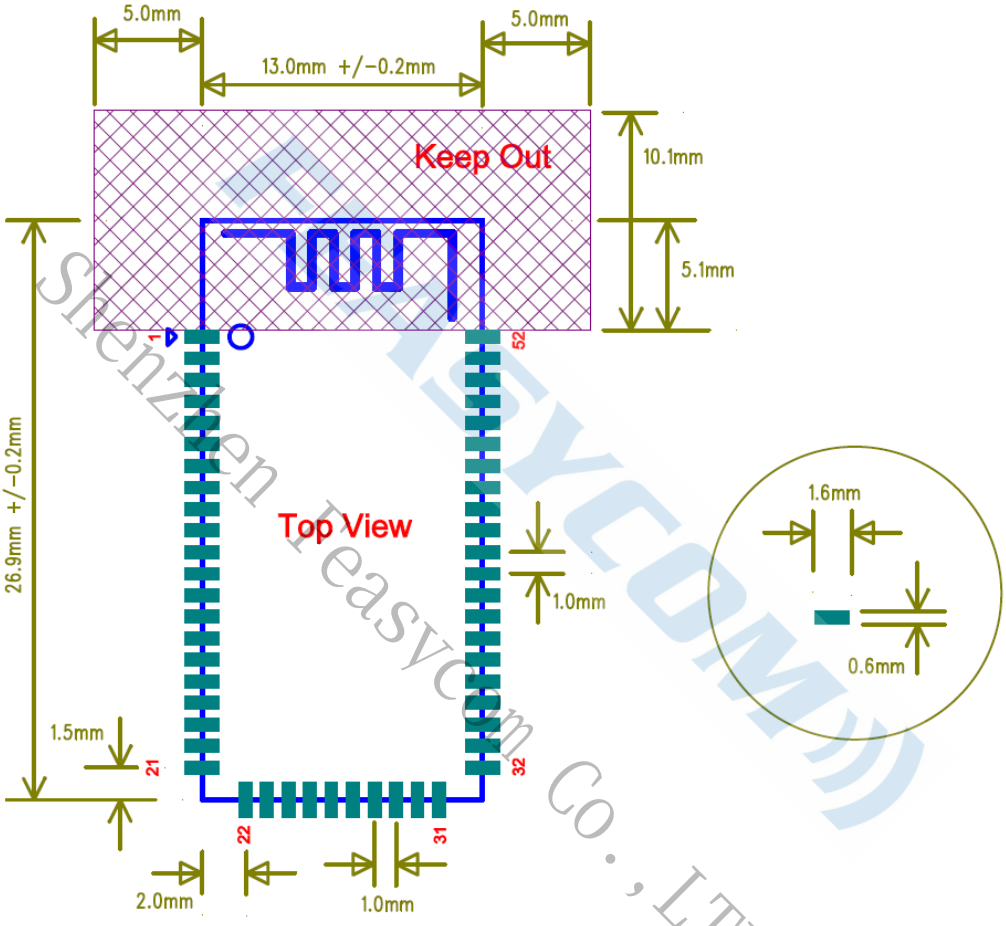

Figure 8-1：FSC-BT1032C footprint Layout Guide (Top View)

9 HARDWARE INTEGRATION SUGGESTIONS

9.1 Soldering Recommendations

FSC-BT1032C is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

9.2 Layout Guidelines(Internal Antenna)

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.

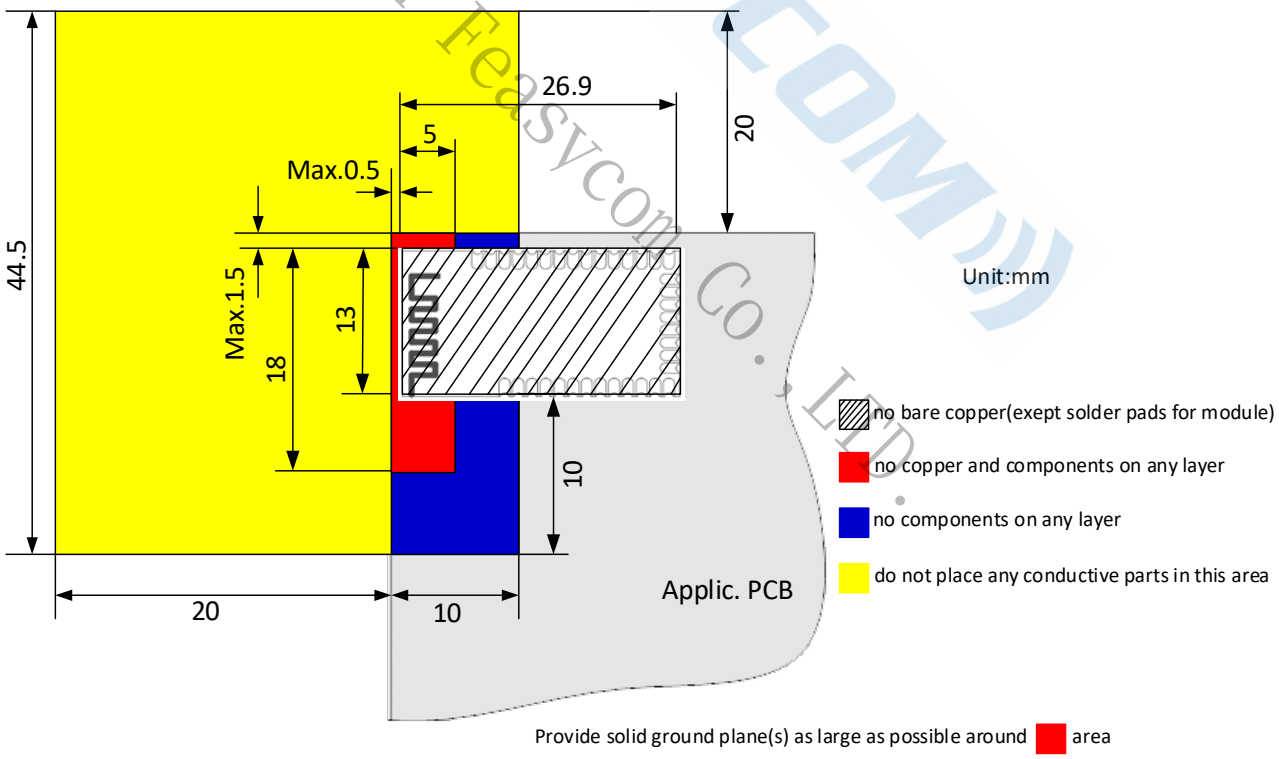

Figure 9-2: Restricted Area (Design schematic, for reference only. Unit: mm)

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid

problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

9.3 Layout Guidelines(External Antenna)

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

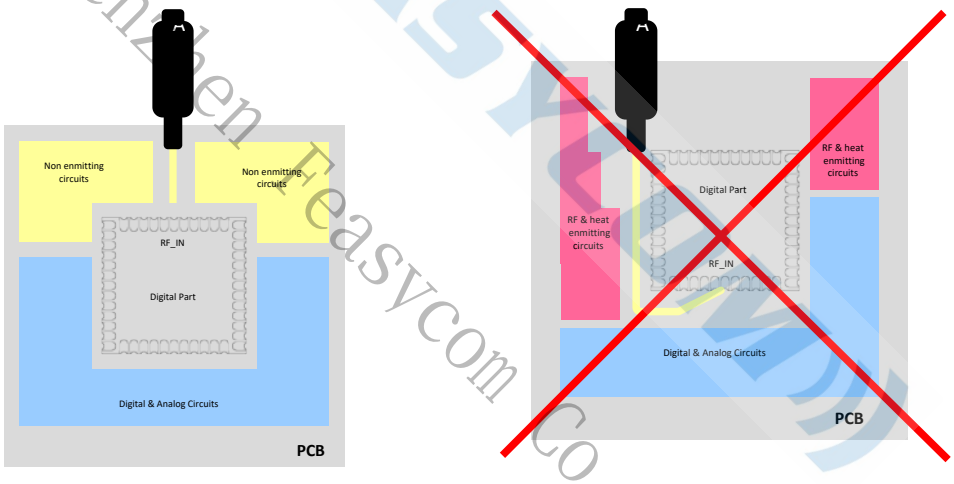

Figure 9-3: Placement the Module on a System Board

9.3.1 Antenna Connection and Grounding Plane Design

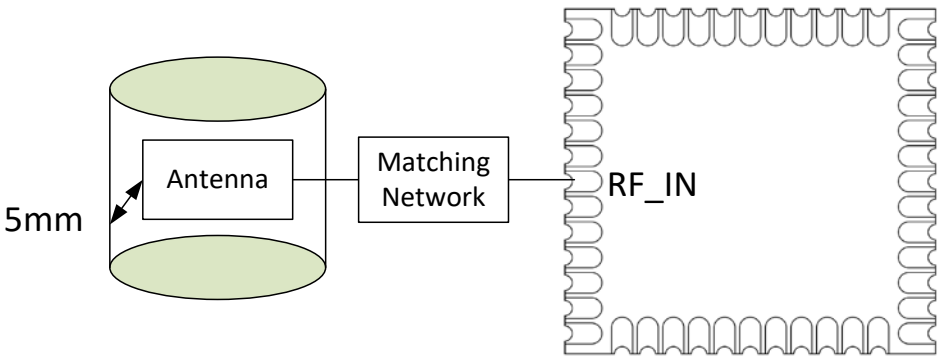

Figure 9-31-0: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

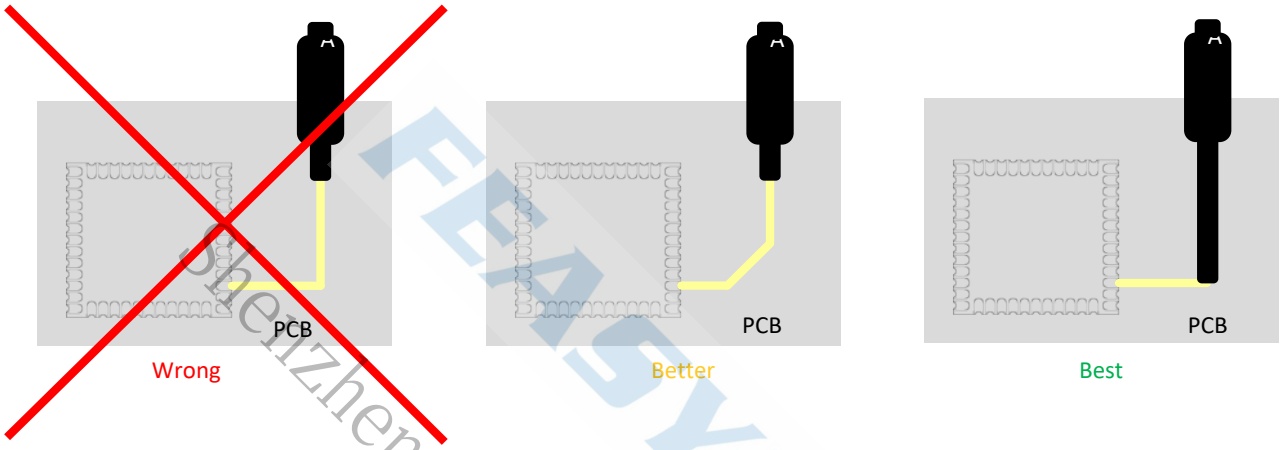

Figure 9-31-1: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

10 PRODUCT PACKAGING INFORMATION

10.1 Default Packing

Figure 10-1: Tray Dimension: 140mm * 265mm Tray vacuum

10.2 Packing box(Optional)

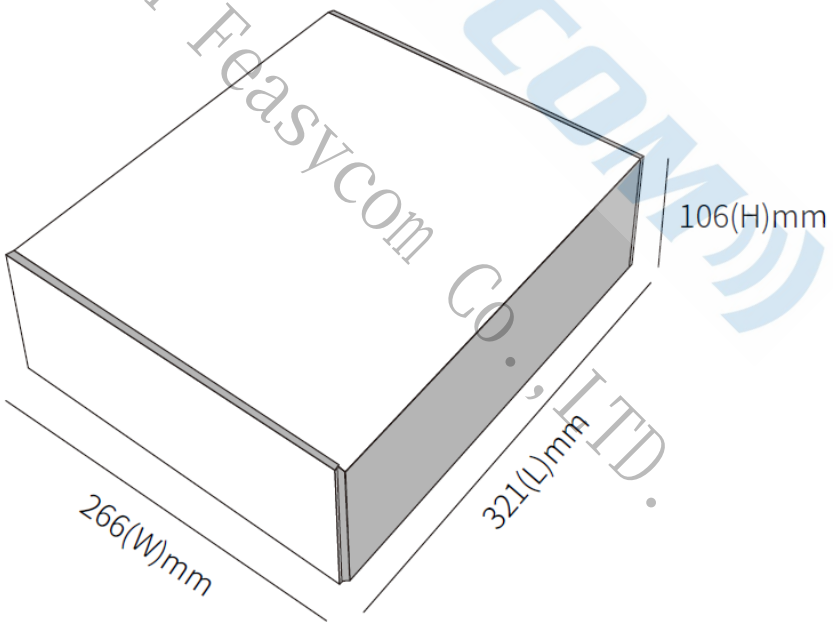

Figure 10-2: Packing box(Optional)

** If other packing is required, please confirm with the customer*

** Packing: 1000pcs per carton (Minimum packing quantity)*

** The outer packing size is for reference only, please refer to the actual size*

11 APPLICATION SCHEMATIC