FSC-BW256

Wi-Fi 6 + BT 5.0 SoC Module Datasheet

Version 1.2

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Revision History

Version	Data	Notes	
1.0	2021/12/02	Initial Version	Jiecai
1.1	2023/3/21	Change the pin description	Mo
1.2	2023/6/13	Version updates	Mo

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1. INTRODUCTION

Overview

FSC-BW256 module adopts a high-performance SOC, it's an industry's leading WIFI6 / BT5.0 dual-mode single chip. While supporting all the indicators of WIFI6, the power consumption is the lowest in the industry. FSC-BW256
integrates Cortex-M4F CPU at the same time, the main frequency can reach 480MHz. With the help of the internal integrated 992KB SRAM, 752KB ROM and up to 128Mbits on-chip SPI flash memory, it provides users with powerful hardware support and can be used for secondary development. FSC-BW256 has a wealth of peripheral interfaces that can be used for control and data transmission through SPI / SDIO / I2C / UART, and can be quickly applied to any microcontroller-based design.

FSC-BW256 module supports the standard IEEE802.11 b/g/n/a/ac/ax protocol and the complete TCP/IP protocol stack. Users can use this module to add networking functions to existing equipment, or build an independent network controller.

FSC-BW256 module provides maximum practicability at the lowest cost, providing unlimited possibilities for Wi-Fi function embedding in other systems.

WiFi Features

- CMOS single-chip fully-integrated RF, Modem and MAC
- Wi-Fi 6 support 2.4GHz/5GHz Frequency band
- The highest data rate is 286.8Mbps@TX and 229.4Mbps@RX, and the bandwidth is 20/40MHz
- RX sensitivity under 11b 1M mode -98dBm
- Tx power up to 20dBm in 11b mode, up to 18dBm in HT/VHT/HE40 MCS7 mode
- Support STA, AP, Wi-Fi Direct mode at the same time
- Support STBC, beamforming
- Support Wi-Fi6 TWT
- Support two NAVs, buffer report, space reuse, Multi-BSSID, power saving in PPDU
- Support LDPC
- Support MU-MIMO, OFDMA
- Support DCM, medium code, UORA
- Support WEP / WPA / WPA2 / WPA3-SAE Personal, MFP Frequency band

BT 5.0 Features

- Supports all the mandatory and optional features of Bluetooth 2.1+EDR/3.0/4.x/5
- Supports advanced master and slave topologies

CPU Features

- Integrated Cortex-M4F CPU with MPU and FPU
- CPU speed up to 480Mhz
- On-chip memory includes 992KB SRAM and 752KB ROM
- Supports SDIO/SPI/USB2.0
- Integrated hardware crypto accelerator AES/RSA/HASH/ECC
- Integrated True Random Number Generator (TRNG)
- Support external OPI SDR/DDR PSRAM
- Integrated 128mbits SPI flash
- Integrated UART/I2S/I2C/PWM/SPI/SDMMC
- Integrated watchdog
- Support freeRTOS

Application

- IoT device
- Wireless device

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Module picture as below showing

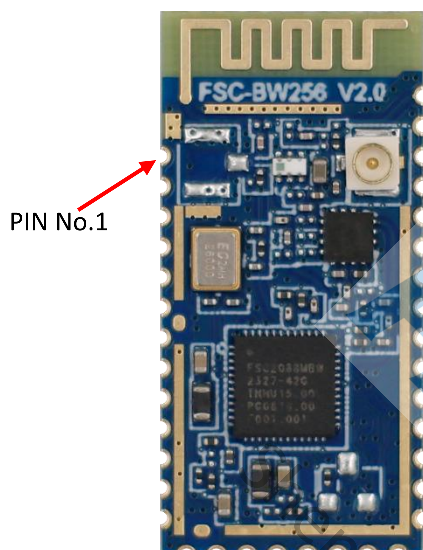

Figure 1: FSC-BW256 V2.0 Picture

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2. General Specification

Table 1: General Specifications

Categories	Features	Implementation
Bluetooth		
Bluetooth Standard		Bluetooth V5.0 LE & BR/EDR
Frequency Band		2402MHz~2480MHz
Interface		UART
WIFI		
WiFi Standard		802.11 a/b/g/n/ac/ax
Frequency Band		2412MHz~2484MHz /4900MHZ~5925MHz
Interface		UART/SPI /USB/SDIO
General		
Size		13mm × 26.9 mm ×2.2mm
Operating temperature		-20°C ~+80°C
Storage temperature		-40°C ~+85°C
VDD_3V3		3V ~ 3.6V
VDD_IO		1.8V ~ 3.3V
Miscellaneous	Lead Free	Lead-free and RoHS compliant
	Warranty	One Year
Humidity		10% ~ 90% non-condensing
MSL grade:		MSL 3
ESD grade:		Human Body Model: Pass ±2000 V, all pins Charge device model: Pass ±400 V, all pins

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3. HARDWARE SPECIFICATION

3.1 Block Diagram and PIN Diagram

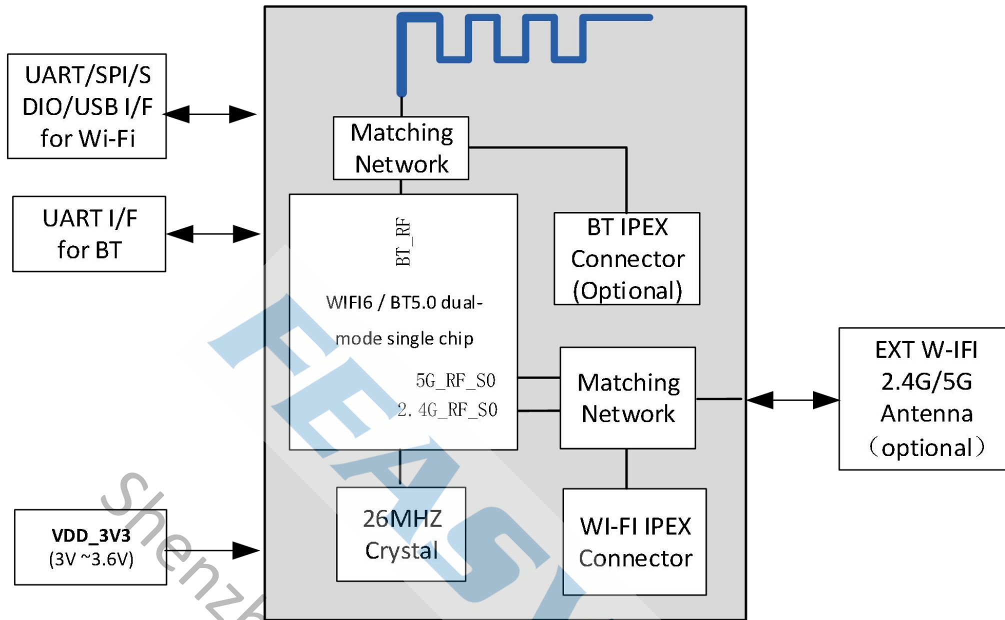

Figure 2: Block Diagram

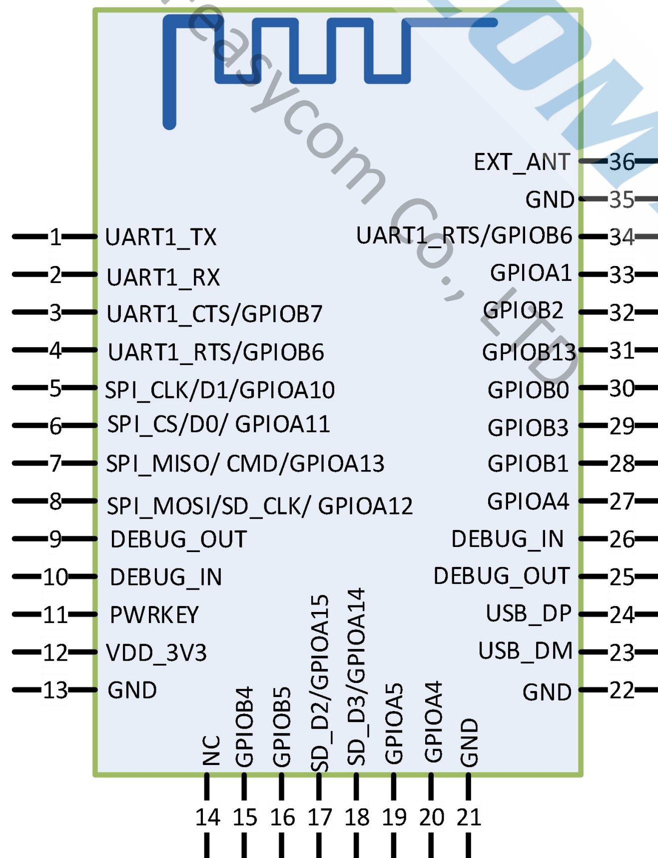

Figure 3: FSC-BW256 PIN Diagram (Top View)

3.2 PIN Definition Descriptions

Table 2: Pin definition

Pin	Pin Name	Type	Pin Descriptions	Notes
1	UART1_TX	O	UART Data output	
2	UART1_RX	I	UART Data input	
3	UART1_CTS/GPIOB7	I/O	Programmable input/output line Alternative Function 1: UART Clear to Send (active low)	
4/34	UART1_RTS/GPIOB6	I/O	Programmable input/output line Alternative Function 1: UART Request to Send (active low)	
5	SPI_CLK/D1/GPIOA10	I/O	SPI_CLK Alternative Function 1: SDIO_ D1 Alternative Function 2: Programmable input/output line	
6	SPI_CS/D0/ GPIOA11	I/O	SPI_CS Alternative Function 1: SDIO_ D0 Alternative Function 2: Programmable input/output line	
7	SPI_MISO/ CMD/GPIOA13	I/O	SPI_MISO Alternative Function 1: SDIO_ CMD Alternative Function 2: Programmable input/output line	
8	SPI_MOSI/SD_CLK/ GPIOA12	I/O	SPI_MOSI Alternative Function 1: SD_CLK Alternative Function 2: Programmable input/output line	
9/25	DEBUG_OUT	I/O	Debug Interface (Data OUT)	
10/26	DEBUG _IN	I/O	Debug Interface (Data IN)	
11	PWRKEY	I	Module power-on pin, power-on = 1; power-off = 0; There is a 100K resistor inside the module, which is pulled up to VDD_3V3	
12	VDD_3V3	VDD	Power supply	
13	GND	VSS	Power Ground	
14	NC			
15	GPIOB4	I/O	Programmable input/output line	
16	GPIOB5	I/O	Programmable input/output line	
17	SD_D2/GPIOA15	I/O	SDIO_D2 Alternative Function 1: Programmable input/output line	
18	SD_D3/GPIOA14	I/O	SDIO_D3 Alternative Function 1: Programmable input/output line	
19	GPIOA5	I/O	Programmable input/output line	
20/27	GPIOA4	I/O	Programmable input/output line	
21	GND	VSS	Power Ground	
22	GND	VSS	Power Ground	
23	USB_DM	I/O	USB data D- Hang in the air when not in use, no need to connect	
24	USB_DP	I/O	USB data D+ Hang in the air when not in use, no need to connect	
28	GPIOB1	I/O	Programmable input/output line	
29	GPIOB3	I/O	Programmable input/output line	
30	GPIOB0	I	Programmable input line	
31	GPIOB13	I/O	Programmable input/output line	
32	GPIOB2	I/O	Programmable input/output line	
33	GPIOA1	I/O	Programmable input/output line	
35	GND	VSS	RF Ground	
36	EXT_ANT	O	BT&WIFI 2.4G radio frequency	

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WiFi 5G radio frequency（optional）

5. ELECTRICAL CHARACTERISTICS

5.1 Recommended Operating Conditions

Table 3: Recommended Operating Conditions

Parameter	Min	Type	Max	Unit
VDD_3V3	3	3.3	3.6	V
VDD_IO	1.8	3.3	--	V
Operating temperature (T_A)	-20	27	+80	°C
Storage temperature (T_{stg})	-40	27	+85	°C
High-level input voltage	0.7 X VDD_IO		VDD_IO	V
Low-level input voltage	0		0.3 X VDD_IO	V

5.2 Power Consumption

Table 4: Power Consumption :

Internal Pull Resistor	Voltage	Power Consumption(mA)(Max)
VDD_3V3	3.3V	500
VDD_IO	3.3V	-
Testing Condition:	2.4GHz Tx MCS0 6.5Mbps	

FSC-BW256 Module Power Consumption:
500mA @ VDD_3V3 (Maximum)

Suggest customer design power capacity are 800mA@VDD_3V3 for FSC-BW256 Module.

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6. MSL & ESD

Table 5: MSL and ESD

Parameter	Value
MSL grade:	MSL 3
ESD grade	**Electrostatic discharge**
ESD – Human-body model (HBM) rating, JESD22-A114-F (Total samples from one wafer lot)	Pass ±2000 V, all pins
ESD – Charge-device model (CDM) rating, JESD22-C101-D (Total samples from one wafer lot)	Pass ±400 V, all pins

7. RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccate (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the below and follow instructions specified by IPC/JEDEC J-STD-033.

Note: The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the below , the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccate and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60%RH.

Notice (注意) :

Feasycom module must use Step-Stencil, suggestion using the stencil thickness about 0.16-0.2mm, it could be modify with the product.

使用我司模块，须使用阶梯钢网，建议阶梯钢网厚度0.16-0.20mm，可根据自己产品适应性，进行相应调整.

Table 6: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Feasycom surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

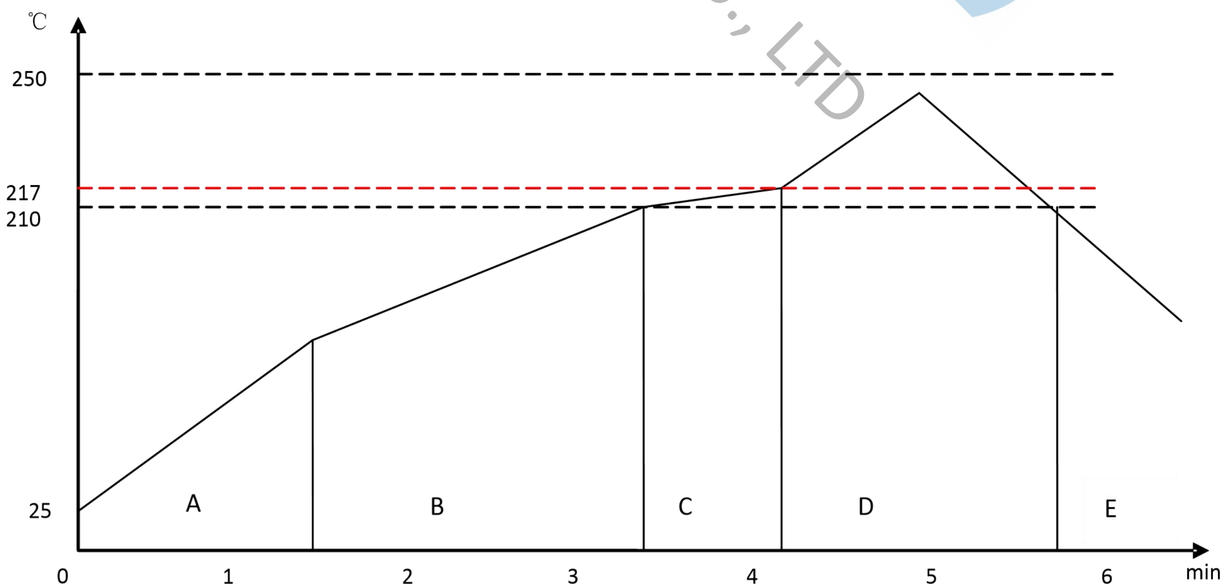

Figure 4: Typical Lead-free Re-flow

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Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

Equilibrium Zone 2 (C) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

8. MECHANICAL DETAILS

8.1 Mechanical Details

- Dimension: 13mm(W) x 26.9mm(L) x 2.2mm(H) Tolerance: ±0.2mm
- Module size: 13mm X 26.9mm Tolerance: ±0.2mm
- Pad size: 1mmX0.8mm Tolerance: ±0.2mm
- Pad pitch: 1.5mm Tolerance: ±0.1mm

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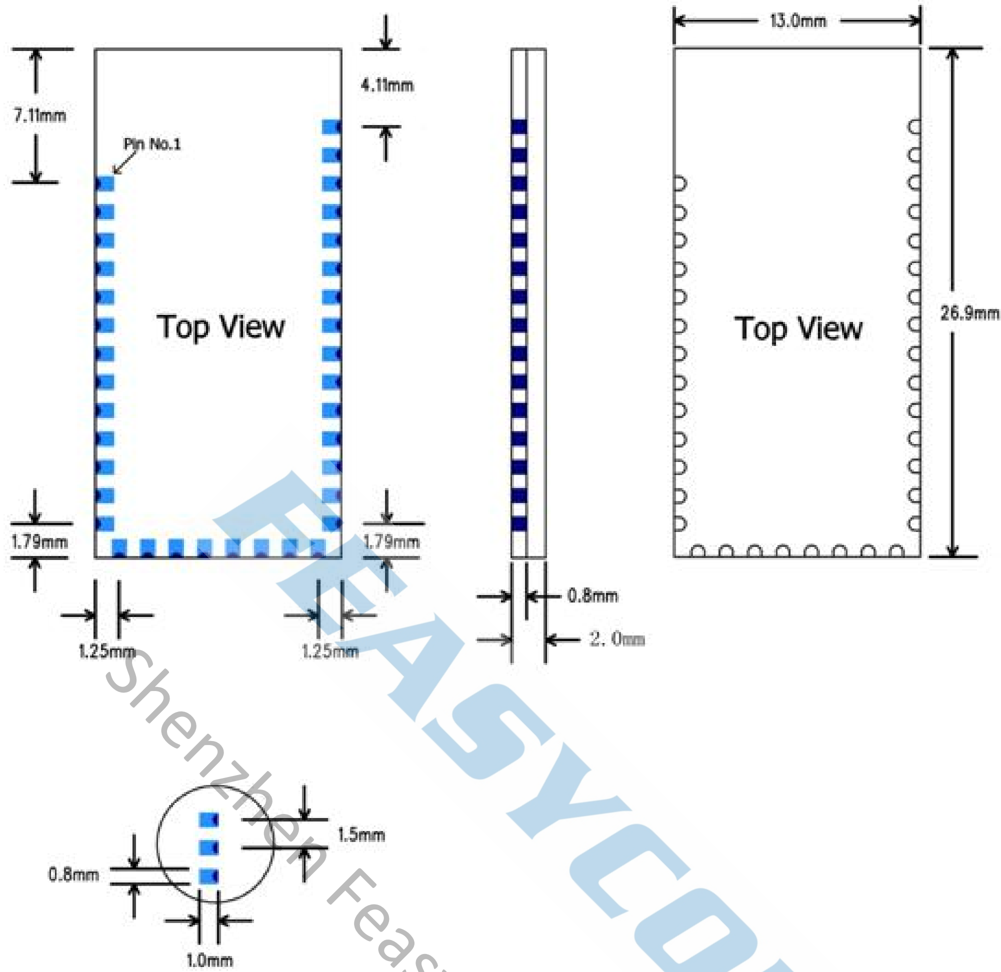

Figure 5: FSC-BW256 footprint Layout Guide (Top View)

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9. HARDWARE INTEGRATION SUGGESTIONS

9.1 Soldering Recommendations

FSC-BW256 is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

9.2 Layout Guidelines(Internal Antenna)

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.

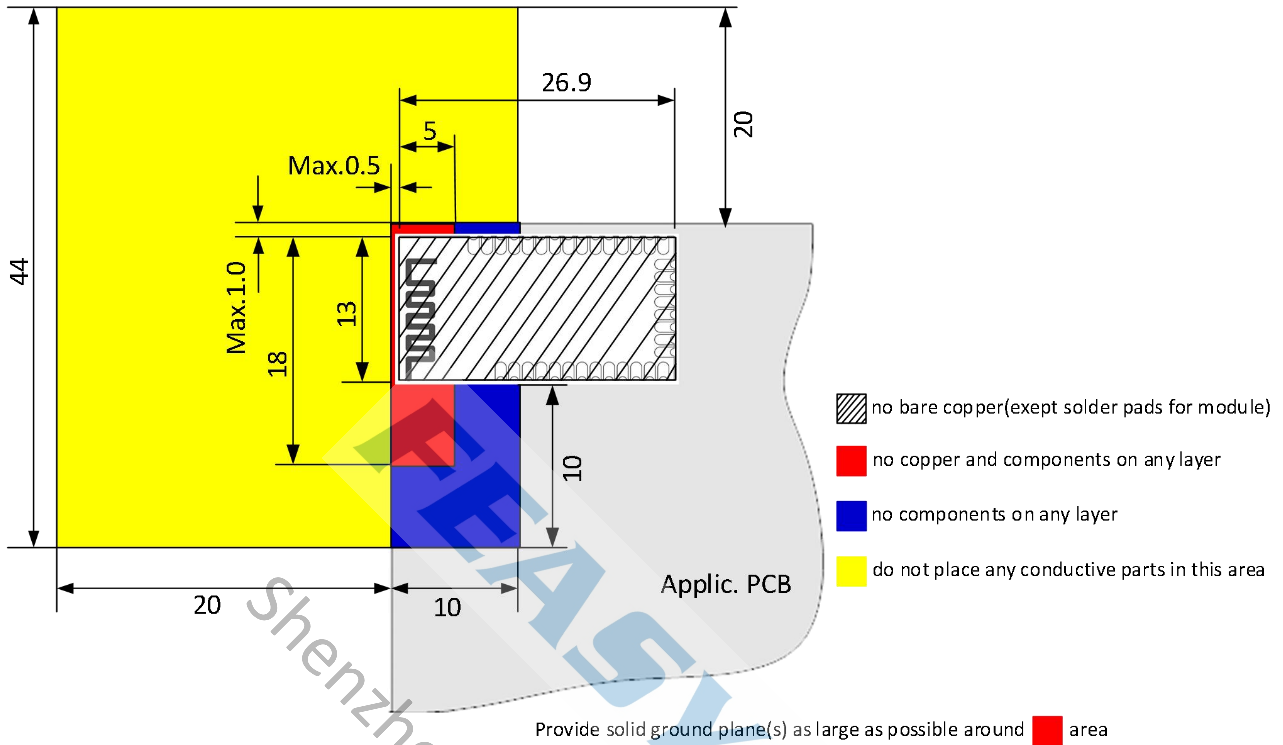

Figure 6: Restricted Area (Design schematic, for reference only. Unit: mm)

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

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9.3 Layout Guidelines(External Antenna)

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

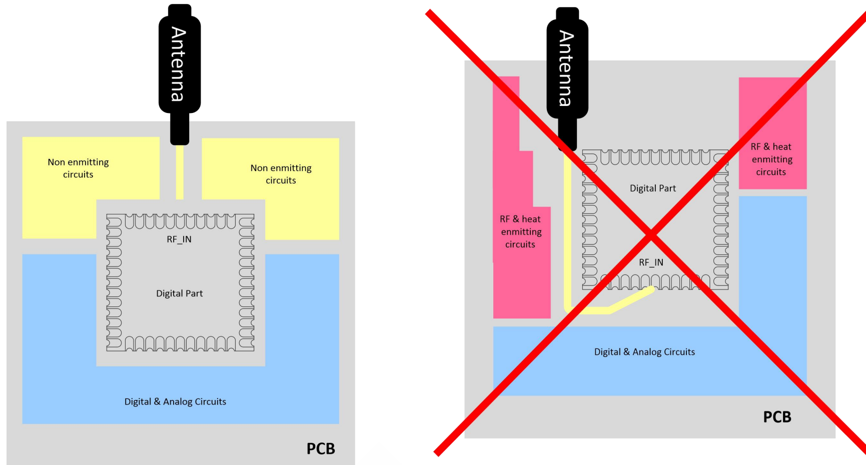

Figure 7: Placement the Module on a System Board

9.3.1 Antenna Connection and Grounding Plane Design

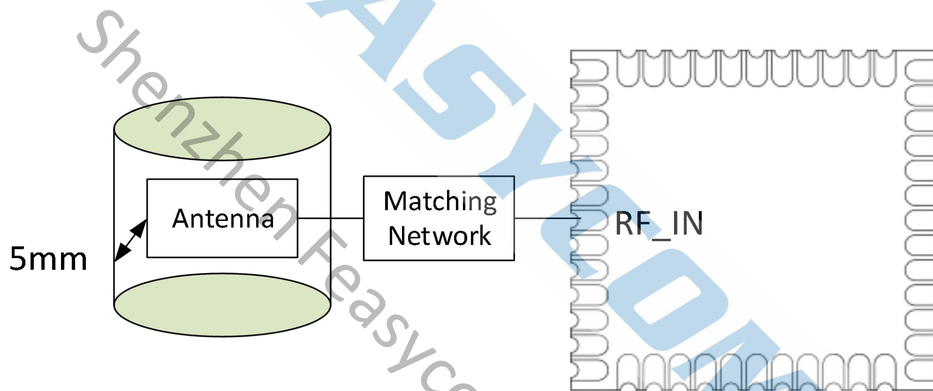

Figure 8: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

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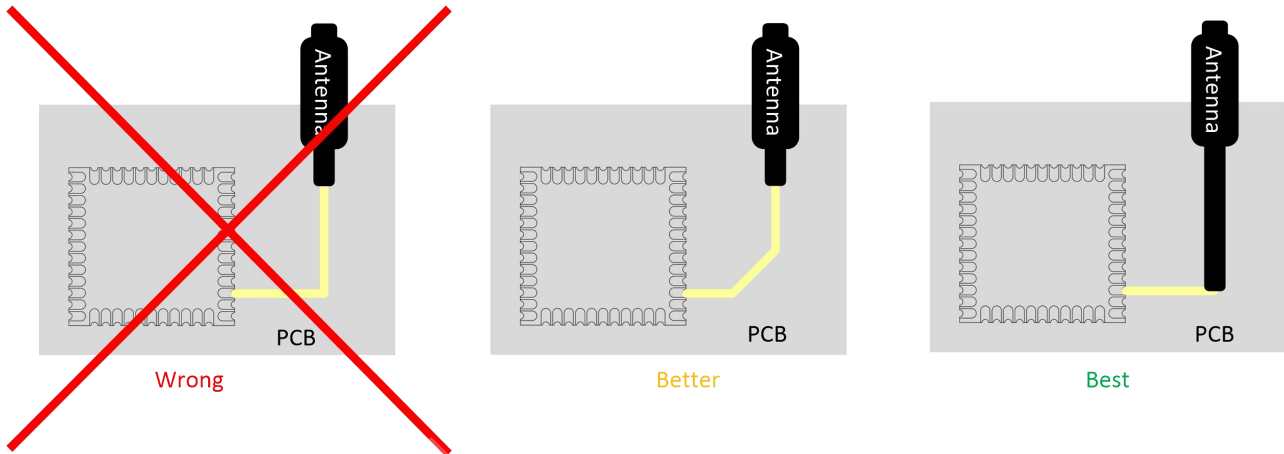

Figure 9: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

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9.4 SDIO Lines Layout Guideline

The following SDIO line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive 8mA.

SDIO_CMD_WL

SDIO_CLK_WL

SDIO_D0_WL ~ SDIO_D3_WL

The route length of these signals be less than 15 cm and the line impedance be less than 50Ω

9.5 HCI Lines Layout Guideline

The following HCI line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive 4 ~ 8mA

HCI_RX_BT

HCI_TX_BT

HCI_CTS_BT

HCI_RTS_BT

The route length of these signals be less than 15 cm and the line impedance be less than 50Ω

9.6 Power Trace Lines Layout Guideline

VDD_3V3 Trace Width: 40mil

9.7 Ground Lines Layout Guideline

A Complete Ground in Ground Layer.

Add Ground Through Holes to FSC-BW256 Module Ground Pads

Decoupling Capacitors close to FSC-BW256 Module Power and Ground Pads

10. PRODUCT PACKAGING INFORMATION

10.1 Default Packing

a, Tray vacuum

b, Tray Dimension: 180mm * 195mm

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Figure 10: Tray vacuum

10.2 Packing box(Optional)

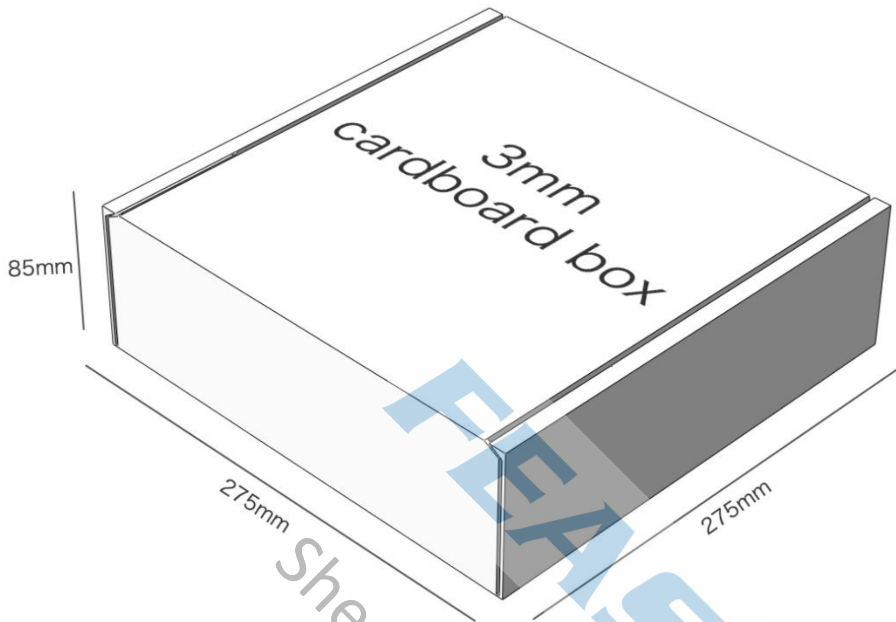

Figure 11: Packing box

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11. APPLICATION SCHEMATIC

The frequency band of the antena must support 2.4GHZ and 5GHZ

50 Ohm Transmission Line

USRT Interface

DUBUG_USRT

POWER ON=1
POWER OFF=0

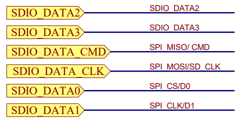
WIFI work Status Indicaror Light

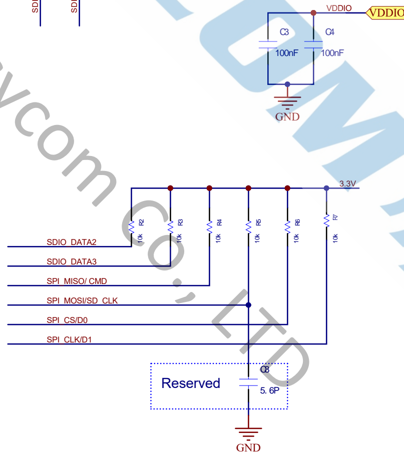
BT work Status Indicaror Light

90 ohm impedance Difference line

Two interfaces Two choose one

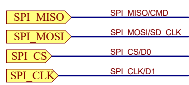
SDIO Interface
50 ohm impedance control and equal line



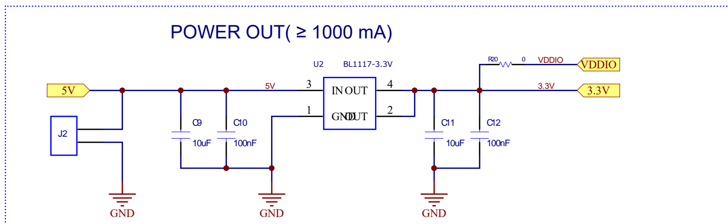


Reserved

SPI Interface



POWER OUT(≥ 1000 mA)



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