



FSC-BT686

Bluetooth Version 5.0 Module Datasheet

Version 1.5

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Revision History

Version	Date	Notes	
1.0	2019/03/09	Initial Version	Fish
1.1	2019/04/03	Update the application circuit diagram and Pin 29 needs to be pulled up.	Fish
1.2	2019/07/22	Update the 16 and 17 pin definitions and application circuit diagrams, modify the shield cover	Fish
1.3	2019/08/30	Update voltage range	Fish
1.4	2019/10/10	Increase the certification directory (SRRC)	Fish
1.5	2020/04/30	Increase power consumption parameters	Fish

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Contents

1. INTRODUCTION	4
2. GENERAL SPECIFICATION	5
3. HARDWARE SPECIFICATION	6
3.1 BLOCK DIAGRAM AND PIN DIAGRAM	6
3.2 PIN DEFINITION DESCRIPTIONS	7
4. PHYSICAL INTERFACE	8
4.1 POWER SUPPLY	8
4.2 RESET	8
4.3 GENERAL PURPOSE ANALOG IO	9
4.4 GENERAL PURPOSE DIGITAL IO	9
4.5 RF INTERFACE	10
4.6 SERIAL INTERFACES	10
4.6.1 UART	10
4.6.2 I2C Interface	11
4.7 PWM GENERATOR AND CAPTURE TIMER (PWM)	11
5. ELECTRICAL CHARACTERISTICS	12
5.1 ABSOLUTE MAXIMUM RATINGS	12
5.2 RECOMMENDED OPERATING CONDITIONS	12
5.3 INPUT/OUTPUT TERMINAL CHARACTERISTICS	12
5.4 ANALOG CHARACTERISTICS	13
5.4.1 Specifications of 12-bit ADC	13
5.5 I2C DYNAMIC CHARACTERISTICS	13
5.6 POWER CONSUMPTIONS	14
6. MSL & ESD	14
7. RECOMMENDED TEMPERATURE REFLOW PROFILE	14
8. MECHANICAL DETAILS	16
8.1 MECHANICAL DETAILS	16
9. HARDWARE INTEGRATION SUGGESTIONS	17
9.1 SOLDERING RECOMMENDATIONS	17
9.2 LAYOUT GUIDELINES (INTERNAL ANTENNA)	17
9.3 LAYOUT GUIDELINES (EXTERNAL ANTENNA)	18
9.3.1 Antenna Connection and Grounding Plane Design	19
10. PRODUCT PACKAGING INFORMATION	20
10.1 DEFAULT PACKING	20
11. APPLICATION SCHEMATIC	21
11.1 CERTIFICATE PICTURE	21

1. INTRODUCTION

Overview

The FSC-BT686 is a highly integrated Bluetooth module which integrates baseband, radio, small form factor, external antenna interface and flash memory. It meets the Bluetooth Version 5.0 specification. For MESH equipment applications, the embedded 4Mbit flash is flexible and allows for custom software development.

Features

- Bluetooth V5.0
- Embedded 32-bit MCU
- Embedded 4Mbit Flash
- 64KB SRAM
- UART programming and data interface (baudrate can up to 921600bps)
- UART/I2C/SPI/PWM control interfaces
- Transmit power: 9.5dBm
- Receiving sensitivity: -94dBm
- Postage stamp sized form factor
- Support External Antenna
- Support I-PEX Antenna
- RoHS compliant
- Power Consumption In Sleep Mode (VDD_3V3 at 3.3V)
 - Discoverable: 2.80mA
 - LE Connection: 931.55uA
- Power Consumption In Working Mode (VDD_3V3 at 3.3 V)
 - Discoverable: 9.65mA
 - LE Connection: 8.36mA
 - LE Connection @ 115200bps: 8.49mA

Application

- Remote controller
- SIG Mesh

Module picture as below showing

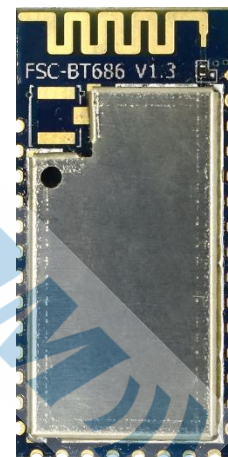


Figure 1: FSC-BT686 Picture

2. General Specification

Table 1: General Specifications

Categories	Features	Implementation
Wireless Specification	Bluetooth Version	Bluetooth V5.0
	Bluetooth Chip	AIROHA AB1611N
	Frequency	2.402 - 2.480 GHz
	Transmit Power	+9.5 dBm (Maximum)
	Receive Sensitivity	-94 dBm@0.1%BER (Typical)
Host Interface and Peripherals	UART Interface	TX,RX,CTS,RTS
		General Purpose I/O
		Default 115200,N,8,1
	GPIO	Baudrate support from 1200 to 921600
		5, 6, 7, 8 data bit character
		22 (maximum – configurable) lines
	I2C Interface	O/P drive strength (4 mA)
		Pull-up resistor (33 KΩ) control
		Read pin-level
	ADC Interface	1 (configurable from GPIO total). Up to 400 kbps
		Analog input voltage range: 0~ 3.3V
	PWM	Supports single 12-bit ADC conversion
		1 channels (configured from GPIO total)
1 General-Purpose Timer Modules		
Profiles	Classic Bluetooth	No Support
	Bluetooth Low Energy	GATT Client & Peripheral - Any Custom Services
Maximum Connections	Classic Bluetooth	No Support
	Bluetooth Low Energy	1 Clients
FW upgrade		Via UART
Supply Voltage	Supply	1.9-3.6V
		Max Peak Current(TX current @ +9.5dBm): 20.29mA
		Max Peak Current(RX current @ 1Mbps): 4.76mA
		Sleep 4uA
Power Consumption		Deep Sleep 0.5uA
	Dimensions	13mm X 26.9mm X 2.0mm; Pad Pitch 1.5mm
Environmental	Operating	-40°C to +105°C
	Storage	-65°C to +150°C
Miscellaneous	Lead Free	Lead-free and RoHS compliant
	Warranty	One Year
Humidity		10% ~ 90% non-condensing
MSL grade:		MSL 3
ESD grade:		Human Body Model: Class-2 ; Machine Model: Class-B

3. HARDWARE SPECIFICATION

3.1 Block Diagram and PIN Diagram

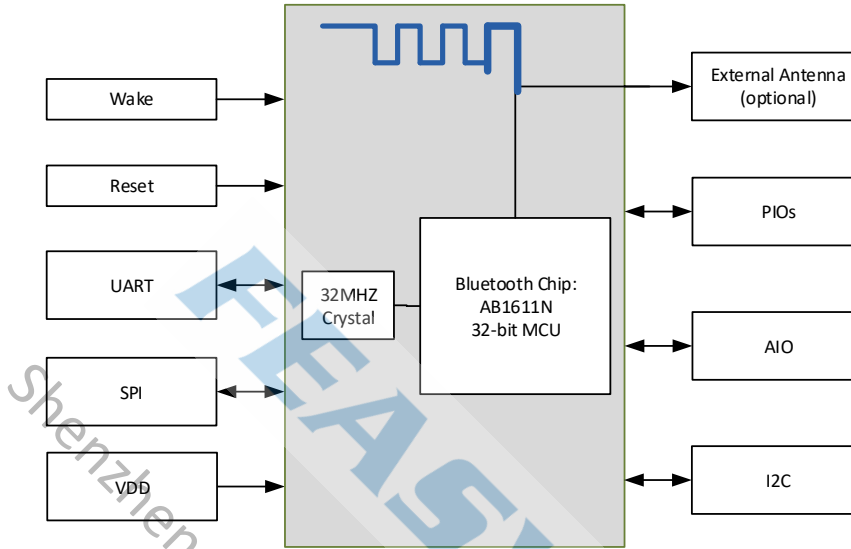


Figure 2: Block Diagram

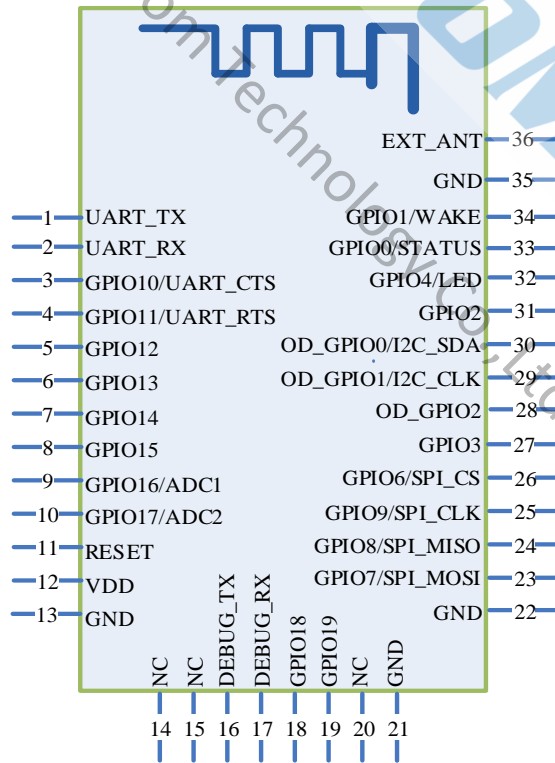


Figure 3: FSC-BT686 PIN Diagram(Top View)

3.2 PIN Definition Descriptions

Table 2: Pin definition

Pin	Pin Name	Type	Pin Descriptions	Notes
1	UART_TX	O	UART data output	
2	UART_RX	I	UART data input	
3	GPIO10/UART_CTS	I/O	UART clear to send active low Alternative Function: Programmable input/output line	Note 1
4	GPIO11/UART_RTS	I/O	UART request to send active low Alternative Function: Programmable input/output line	Note 1
5	GPIO12	I/O	Programmable input/output line	
6	GPIO13	I/O	Programmable input/output line	
7	GPIO14	I/O	Programmable input/output line	
8	GPIO15	I/O	Programmable input/output line.	
9	GPIO16/ADC1	I/O	Programmable input/output line Alternative Function 1: Analogue programmable I/O line. Alternative Function 2: Host MCU change UART transmission mode.	Note 1
10	GPIO17/ADC2	I/O	Programmable input/output line Alternative Function 1: Analogue programmable I/O line. Alternative Function 2: Host MCU disconnect bluetooth.	Note 1
11	RESET	I	External reset input: Active LOW, with an inter an internal pull-up Set this pin low reset to initial state	
12	VDD	Vdd	Power supply voltage 1.7V ~ 3.6V	
13	GND	Vss	Power Ground	
14	NC			
15	NC			
16	DEBUG_TX	O	Debug data transmission	
17	DEBUG_RX	I	Debug data reception	
18	GPIO18	I/O	Programmable input/output line	
19	GPIO19	I/O	Programmable input/output line	
20	NC			
21	GND	Vss	Power Ground	
22	GND	Vss	Power Ground	
23	GPIO7/SPI_MOSI	I/O	Programmable input/output line * The I/O port for reuse.	Note 6
24	GPIO8/SPI_MISO	I/O	Programmable input/output line * The I/O port for reuse.	Note 6
25	GPIO9/SPI_CLK	I/O	Programmable input/output line * The I/O port for reuse.	Note 6
26	GPIO6/SPI_CS	I/O	Programmable input/output line * The I/O port for reuse.	Note 6
27	GPIO3	I/O	Programmable input/output line	
28	OD_GPIO2	I/O	Programmable input/output line	

29	OD_GPIO1/IC2_CLK	I/O	Alternative Function: Programmable input/output line Alternative Function: I2C CLK line (Default)	Note 1,3
30	OD_GPIO0/IC2_SDA	I/O	Programmable input/output line Alternative Function: I2C DATA line (Default)	Note 1,3
31	GPIO2	I/O	Programmable input/output line	
32	GPIO4/LED	I/O	Programmable input/output line Alternative Function: LED(Default)	Note 1,4
33	GPIO0/STATUS	I/O	Programmable input/output line Alternative Function: BT Status(Default)	Note 1,2
34	GPIO1/WAKE	I/O	Programmable input/output line Alternative Function: H=Sleep L=Wake up	Note 1
35	GND	Vss	Power Ground	
36	EXT_ANT	O	RF signal output.	Note 5

Module Pin Notes:

Note 1	For customized module, this pin can be work as I/O Interface.
Note 2	BT Status(Default)-- Disconnected: Low Level; Connected: High Level.
Note 3	I2C Serial Clock and Data. Internal pull up.
Note 4	LED(Default)-- Power On: Light Slow Shinning ; Connected: Steady Lighting.
Note 5	By default, this PIN is an empty feet. This PIN can connect to an external antenna to improve the Bluetooth signal coverage. If you need to use an external antenna, by modifying the module on the OR resistance to block out the on-board antenna; Or contact Feasycom for modification.
Note 6	This I / O port is shared with the internal SPI Flash chip. We do not recommend using this pin, floating processing. This pin is only available when the module is not equipped with air-upgrade function.

4. PHYSICAL INTERFACE

4.1 Power Supply

The transient response of the regulator is important. If the power rails of the module are supplied from an external voltage source, the transient response of any regulator used should be 20μs or less. It is essential that the power rail recovers quickly.

4.2 Reset

The module may be reset from several sources: Power-on Reset (POR), Low level on the nRESET Pin (nRST), Watchdog time-out reset (WDT), Low voltage reset (LVR) or Software Reset(SYSRESETREQ, CPU Reset, CHIPRST).

The RESET pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. A reset will be performed between 1.5 and 4.0ms following RESET being active. It is recommended that RESET be applied for a period greater than 5ms.

At reset the digital I/O pins are set to inputs for bi-directional pins and outputs are tri-state. The PIOs have weak pull-

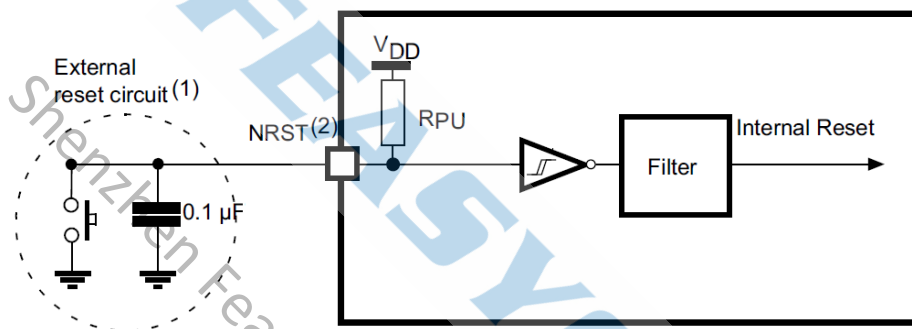
ups.

Table 3: NRST pin characteristics

Parameter	Conditions	Min	Typ	Max	Unit
R_{PU} - Weak pull-up equivalent resistor ⁽¹⁾	$V_{IN} = V_{SS}$	30	40	50	k Ω
$V_{F(NRST)}$ ⁽²⁾ - NRST Input filtered pulse		-	-	100	ns
$V_{NF(NRST)}$ ⁽²⁾ - NRST Input not filtered pulse	$V_{DD} > 2.7V$	300	-	-	ns
T_{NRST_OUT} - Generated reset pulse duration	Internal Reset source	20	-	-	μs

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

2. Guaranteed by design.



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *NRST pin characteristics*. Otherwise the reset is not taken into account by the device.

Figure 4: Recommended NRST pin protection

4.3 General Purpose Analog IO

FSC-BT686 contains One 12-bit successive approximation analog-to-digital converter (ADC) with 1 single-end external input channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

4.4 General Purpose Digital IO

There are 22 general purpose digital IOs defined in the module. All these GPIOs can be configured by software to realize various functions, such as button controls, LED drives or interrupt signals to host controller, etc. Do not connect them if not use.

The I/O type of each I/O pins can be configured by software individually as Input or Push-pull output mode. After the chip is reset, the I/O mode of all pins is input mode with no pull-up and pull-down enable. Each I/O pin has an individual pull-up and pull-down resistor which is about 40 k Ω for VDD and Vss.

4.5 RF Interface

For This Module, the default mode for antenna is external antenna.

The user can connect a 50 ohm antenna directly to the RF port.

- 2402–2480 MHz Bluetooth 5.
- TX output power of +9.5dBm.
- Receiver to achieve maximum sensitivity -94dBm.

4.6 Serial Interfaces

4.6.1 UART

FSC-BT686 provides one channels of Universal Asynchronous Receiver/Transmitters (UART) (Full-duplex asynchronous communications). The UART Controller performs a serial-to-parallel conversion on data received from the peripheral and a parallel-to-serial conversion on data transmitted from the CPU. Each UART Controller channel supports ten types of interrupts.

This is a standard UART interface for communicating with other serial devices. The UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

When the module is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators.

This module output is at 3.3V CMOS logic levels (tracks VCC). Level conversion must be added to interface with an RS-232 level compliant interface.

Some serial implementations link CTS and RTS to remove the need for handshaking. We do not recommend linking CTS and RTS except for testing and prototyping. If these pins are linked and the host sends data when the FSC-BT686 deasserts its RTS signal, there is significant risk that internal receive buffers will overflow, which could lead to an internal processor crash. This drops the connection and may require a power cycle to reset the module. We recommend that you adhere to the correct CTS/RTS handshaking protocol for proper operation.

Table 4: Possible UART Settings

Parameter	Possible Values	
Baudrate	Minimum	1200 baud ($\leq 2\%$ Error)
	Standard	115200bps($\leq 1\%$ Error)
	Maximum	921600bps($\leq 1\%$ Error)
Flow control	RTS/CTS, or None	
Parity	None, Odd or Even	
Number of stop bits	1 or 2	
Bits per channel	5/6/7/8	

When connecting the module to a host, please make sure to follow .

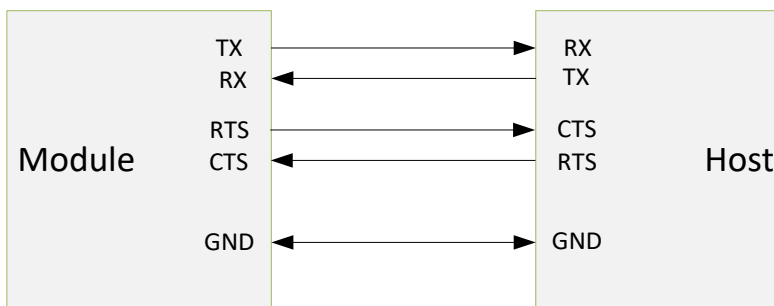


Figure 5: UART Connection

4.6.2 I2C Interface

I2C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I2C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

Data is transferred between a Master and a Slave synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8-bit long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to the following figure for more details about I2C Bus Timing.

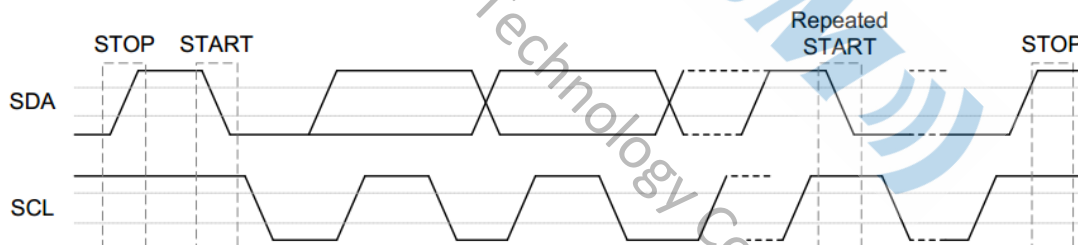


Figure 6: I2C Bus Timing

The device on-chip I2C logic provides the serial interface that meets the I2C bus standard mode specification. The I2C port handles byte transfers autonomously. The I2C H/W interfaces to the I2C bus via two pins: SDA and SCL. Pull up resistor is needed for I2C operation as these are open drain pins. When the I/O pins are used as I2C port, user must set the pins function to I2C in advance.

4.7 PWM Generator and Capture Timer (PWM)

The PWM is designed to generate programmable pulse width of outputs. There is one timer to count cycles of the peripheral clock(PCLK) and can optionally generate interrupts or perform other actions at specified timer values based on 2 set of four match registers. The peripheral clock is provided by the system clock

5. ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

Absolute maximum ratings for supply voltage and voltages on digital and analogue pins of the module are listed below. Exceeding these values causes permanent damage.

The average PIO pin output current is defined as the average current value flowing through any one of the corresponding pins for a 100mS period. The total average PIO pin output current is defined as the average current value flowing through all of the corresponding pins for a 100mS period. The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

Table 5: Absolute Maximum Rating

Parameter	Min	Max	Unit
V _{DD} -V _{SS} - DC Power Supply	-0.3	+3.6	V
V _{IN} - Input Voltage	V _{SS} -0.3	V _{DD} +0.3	V
T _A - Operating Temperature	-40	+105	°C
T _{ST} - Storage Temperature	-65	+150	°C
I _{IO} - Maximum Current sunk by a I/O pin		4	mA
I _{IO} - Maximum Current sourced by a I/O pin		4	mA

5.2 Recommended Operating Conditions

Table 6: Recommended Operating Conditions

Parameter	Min	Type	Max	Unit
V _{DD} -V _{SS} - DC Power Supply	1.9	3.3	3.6	V
V _{IN} - Input Voltage	V _{SS} -0.3	3.3	V _{DD} +0.3	V

5.3 Input/output Terminal Characteristics

Table 7: DC Characteristics

Parameter	Min	Type	Max	Unit
V _{DD} - Operation Voltage	1.9	3.3	3.6	V
V _{SS} - Power Ground	-0.3	-	-	V
V _{DD12} - Core Logic and I/O Buffer Pre-Driver Voltage	1.08	1.2	1.32	V
V _{OH} - High Level Output Voltage	V _{DD} -0.2	-	-	V
V _{OL} - Low Level Output Voltage	-	-	0.2	V
V _{IH} - Input High Voltage	0.7*V _{DD}	-	V _{DD} +0.4	V
V _{IL} - Input Low Voltage	0	-	0.3*V _{DD}	V

5.4 Analog Characteristics

5.4.1 Specifications of 12-bit ADC

Table 8: ADC characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Number of input channels for AIO			1		
Input voltage range		0		3.3	V
Input resistance			300		Kohm
Conversion time		1		256	Us
ENOB	Max sampling rate = 3.9kHz		12		bit
Current consumption			1.5		mA
Integral nonlinearity		-2		2	LSB
Differential nonlinearity		-1		1	LSB

5.5 I2C Dynamic Characteristics

Table 9: I2C Dynamic Characteristics

Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
	Min	Max	Min	Max	
t _{LOW} - SCL low period	4.7	-	1.2	-	uS
T _{HIGH} - SCL high period	4	-	0.6	-	uS
t _{SU;STA} - Repeated START condition setup time	4.7	-	1.2	-	uS
t _{HD;STA} - START condition hold time	4	-	0.6	-	uS
t _{SU;STO} - STOP condition setup time	4	-	0.6	-	uS
t _{BUF} - Bus free time	4.7[3]	-	1.2[3]	-	uS
t _{SU;DAT} - Data setup time	250	-	100	-	uS
t _{HD;DAT} - Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	uS
t _r - SCL/SDA rise time	-	1000	20+0.1CB	300	uS
t _f - SCL/SDA fall time	-	300	-	300	uS
C _b - Capacitive load for each bus line	-	400	-	400	pF

Note:

1. Guaranteed by design, not tested in production.
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I2C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I2C frequency.
3. I2C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

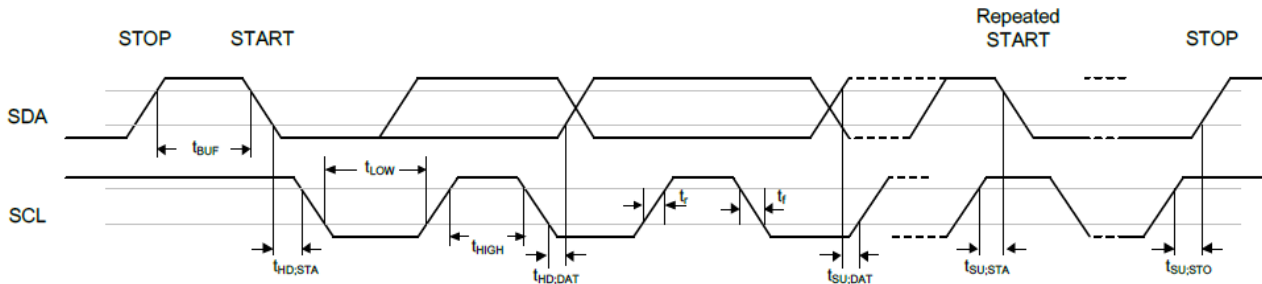


Figure 7: I2C Timing Diagram

5.6 Power consumptions

Table 10: Power consumptions

Parameter	Test Conditions	Type	Unit
Tx current @9.5dBm	VDD=3V, Tx=9.5dBm, LEDs disconnected.	~35	mA
Rx current @1Mbps		4.76	mA
Sleep	VDD=3V, Tx=9.5dBm, LEDs disconnected.	4	uA
Deepsleep	VDD=3V, Tx=9.5dBm, LEDs disconnected.	0.5	uA
Shut down mode	VDD=3V, Tx=9.5dBm, LEDs disconnected.	0.1	uA

6. MSL & ESD

Table 11: MSL and ESD

Parameter	Value
MSL grade:	MSL 3
ESD grade:	Human Body Model: Class-2
	Machine Model: Class-B

7. RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccant (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the below **Table 11** and follow instructions specified by IPC/JEDEC J-STD-033.

Note: The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the below **Table 11**, the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccant and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60%RH.

Table 11: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Feasycom surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

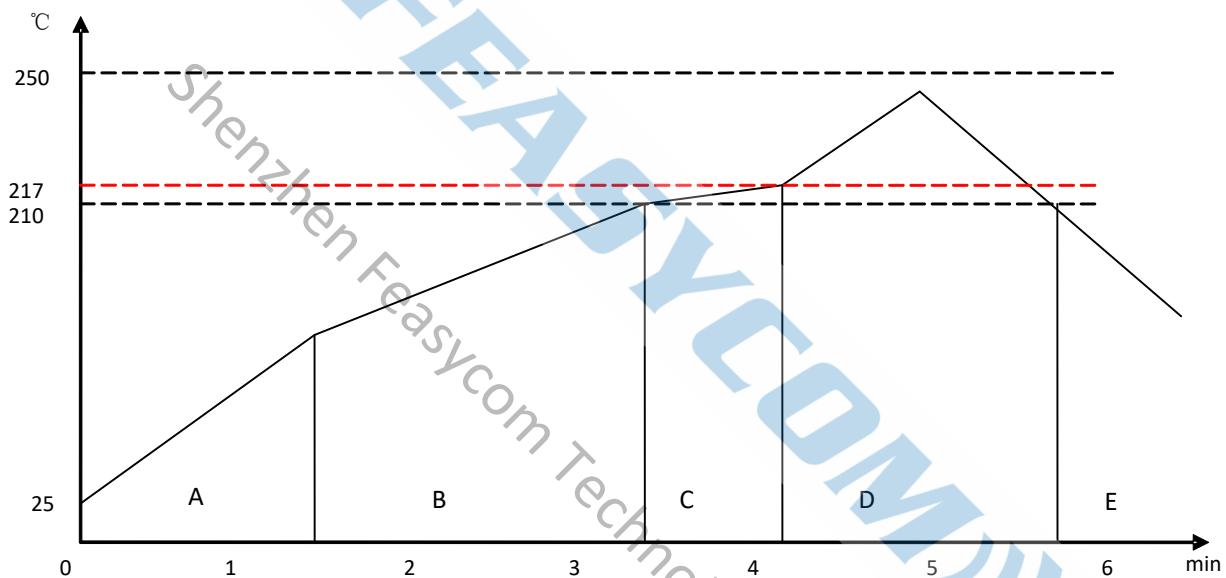


Figure 8: Typical Lead-free Re-flow

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, typically 0.5 – 2 °C/s. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

Equilibrium Zone 2 (C) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

8. MECHANICAL DETAILS

8.1 Mechanical Details

- Dimension: 13mm(W) x 26.9mm(L) x 2.0 mm(H) Tolerance: $\pm 0.1\text{mm}$
- Module size: 13mm X 26.9mm Tolerance: $\pm 0.2\text{mm}$
- Pad size: 1mmX0.8mm Tolerance: $\pm 0.1\text{mm}$
- Pad pitch: 1.5mm Tolerance: $\pm 0.1\text{mm}$

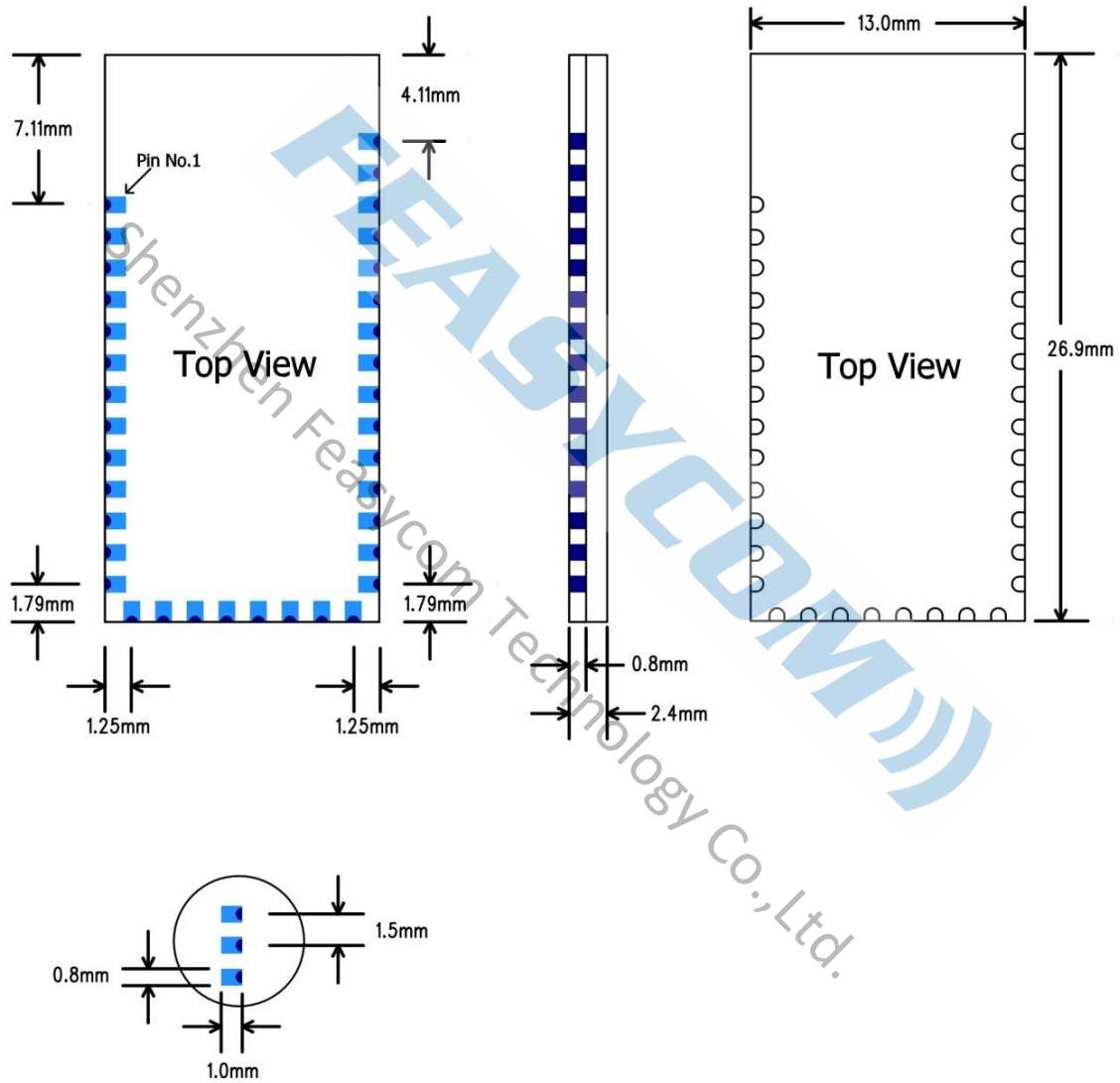


Figure 9: FSC-BT686 footprint

9. HARDWARE INTEGRATION SUGGESTIONS

9.1 Soldering Recommendations

FSC-BT686 is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

9.2 Layout Guidelines(Internal Antenna)

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.

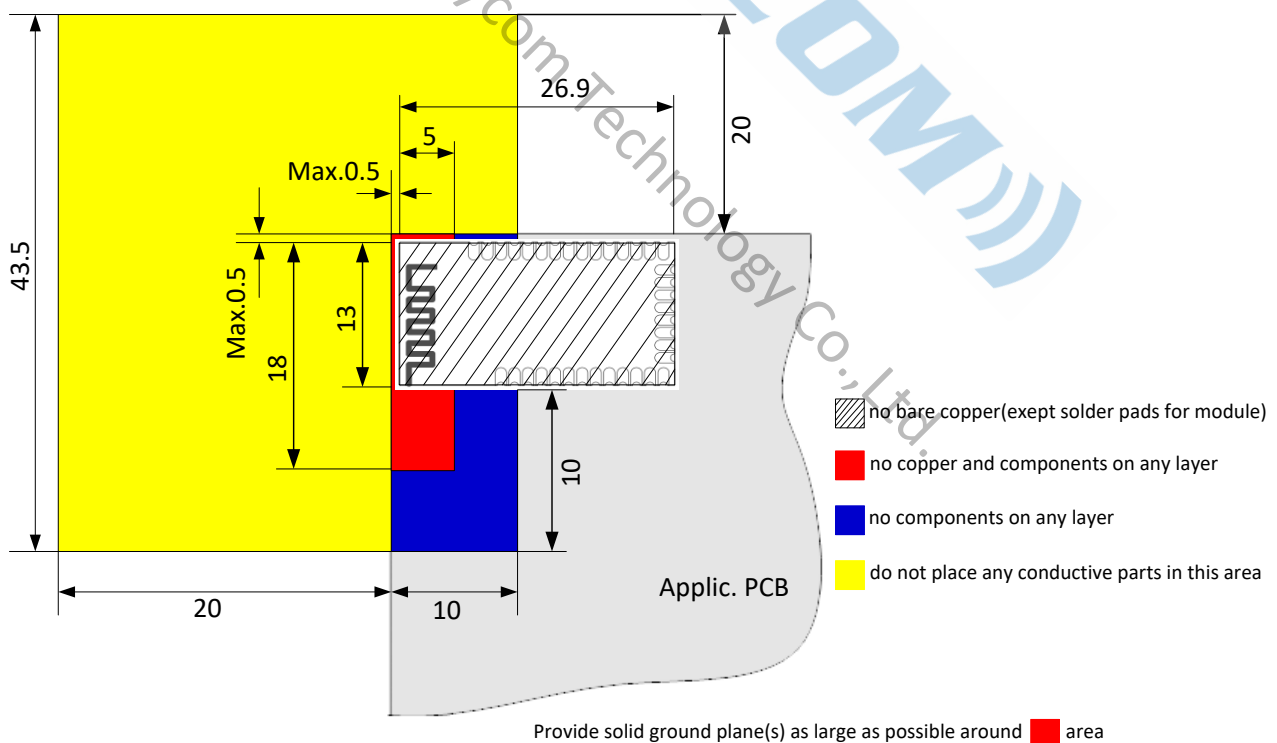


Figure 10: FSC-BT686 Restricted Area

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid problems arising

from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

9.3 Layout Guidelines(External Antenna)

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in **Figure 16** below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

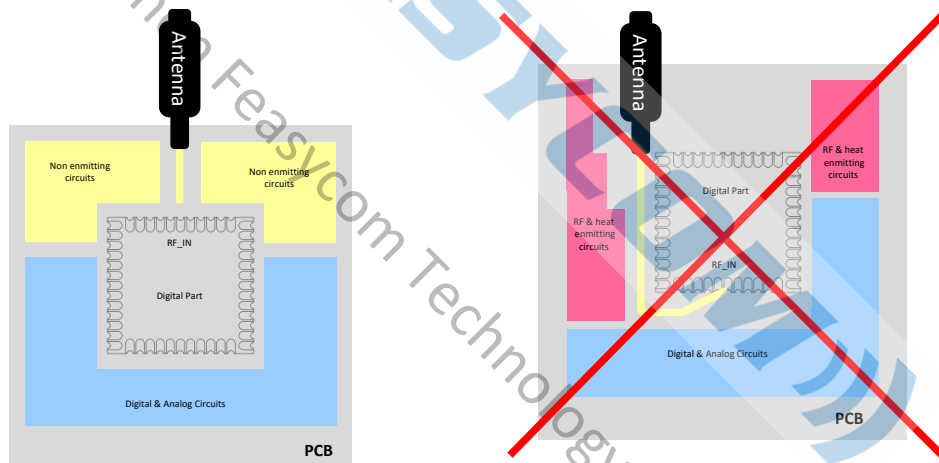


Figure 11: Placement the Module on a System Board

9.3.1 Antenna Connection and Grounding Plane Design

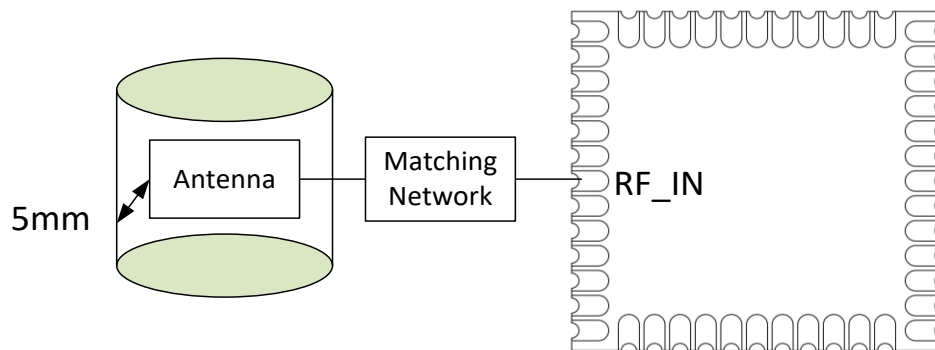


Figure 12: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

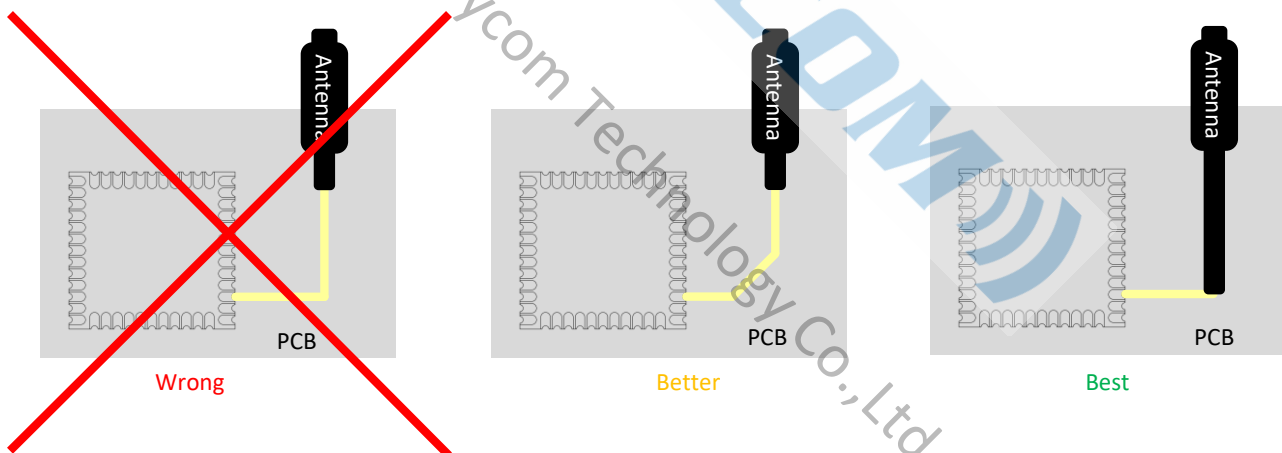


Figure 13: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

10. PRODUCT PACKAGING INFORMATION

10.1 Default Packing

- a, Tray vacuum
- b, Tray Dimension: 180mm * 195mm



Figure 14: Tray vacuum (Image for reference only, subject to actual product)

11. APPLICATION SCHEMATIC

11.1 Certificate picture

Has passed SRRC certification.



12. APPLICATION SCHEMATIC

