FSC-BW150

Bluetooth 5.0 + Wi-Fi 6 Module Datasheet

Version 1.0

Revision History

Version	Data	Notes	
1.0	2021/03/18	Initial Version	jiecai

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1. INTRODUCTION

Overview

FSC-BW150 module adopts a high-performance SoC, it's an industry's leading dual-band Wi-Fi6 / BT5.0 dual-mode single chip. While supporting all the indicators of WIFI6, the power consumption is the lowest in the industry. FSC-BW150 integrates Cortex-M4F CPU at the same time, the main frequency can reach 480MHz. With the help of the internal integrated 992KB SRAM, 752KB ROM and up to 128Mbits on-chip SPI flash memory, it provides users with powerful hardware support and can be used for secondary development. FSC-BW150 has a wealth of peripheral interfaces that can be used for control and data transmission through SPI / SDIO / I2C / UART, and can be quickly applied to any microcontroller-based design.

FSC-BW150 module supports the standard IEEE802.11 b/g/n/a/ac/ax protocol and the complete TCP/IP protocol stack. Users can use this module to add networking functions to existing equipment, or build an independent network controller.

FSC-BW150 module provides maximum practicability at the lowest cost, providing unlimited possibilities for Wi-Fi function embedding in other systems.

Wi-Fi Features

- CMOS single-chip fully-integrated RF, Modem and MAC
- Wi-Fi 6 support 2.4GHz/5GHz Frequency band
- The highest data rate is 286.8Mbps@TX and 229.4Mbps@RX, and the bandwidth is 20/40MHz
- RX sensitivity under 11b 1M mode -98dBm
- Tx power up to 20dBm in 11b mode, up to 18dBm in HT/VHT/HE40 MCS7 mode
- Support STA, AP, Wi-Fi Direct mode at the same time
- Support STBC, beamforming
- Support Wi-Fi 6 TWT
- Support two NAVs, buffer report, spatial reuse, Multi-BSSID, intra-PPDU power save
- Support LDPC
- Support MU-MIMO, OFDMA
- Support DCM, Mid-amble, UORA
- Support WEP / WPA / WPA2 / WPA3-SAE Personal, MFP Frequency band

BT5.0 Features

- Supports all the mandatory and optional features of Bluetooth 2.1+EDR/3.0/4.x/5
- Supports advanced master and slave topologies

CPU Features

- Integrated Cortex-M4F CPU with MPU and FPU
- CPU speed up to 480Mhz
- On-chip memory includes 992KB SRAM and 752KB ROM
- Supports SDIO/SPI/USB2.0
- Integrated hardware crypto accelerator AES/RSA/HASH/ECC
- Integrated True Random Number Generator (TRNG)
- Support external OPI SDR/DDR PSRAM
- Integrated 128mbits SPI flash
- Integrated UART/I2S/I2C/PWM/SPI/SDMMC
- Integrated watchdog

Application

- IoT device
- Wireless device

Module picture as below showing

Figure 1: FSC-BW150 Picture

2. General Specification

Table 1: General Specifications

Categories	Features	Implementation
Bluetooth		
Bluetooth Standard		Bluetooth V5.0 LE & BR/EDR
Frequency Band		2402MHz~2480MHz
Interface		UART
WIFI		
WiFi Standard		802.11 a/b/g/n/ac/ax
Frequency Band		2412MHz~2484MHz /4900MHZ~5925MHz
Interface		SDIO
General		
Size		12mm × 12 mm × 2.2mm
Operating temperature		-20°C ~+80°C
Storage temperature		-40°C ~+85°C
VDD_3V3		2.3V ~ 3.6V
VDD_IO		1.8V ~ 3.6V
Miscellaneous	Lead Free	Lead-free and RoHS compliant
	Warranty	One Year
Humidity		10% ~ 90% non-condensing
MSL grade:		MSL 3
ESD grade:		Human Body Model: Pass ±2000 V, all pins Charge device model: Pass ±400 V, all pins

3. HARDWARE SPECIFICATION

3.1 Block Diagram and PIN Diagram

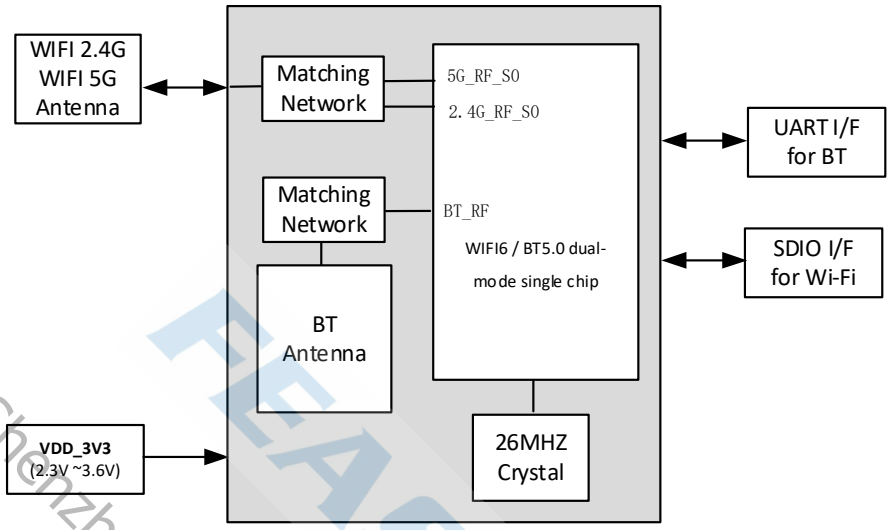


Figure 2: Block Diagram

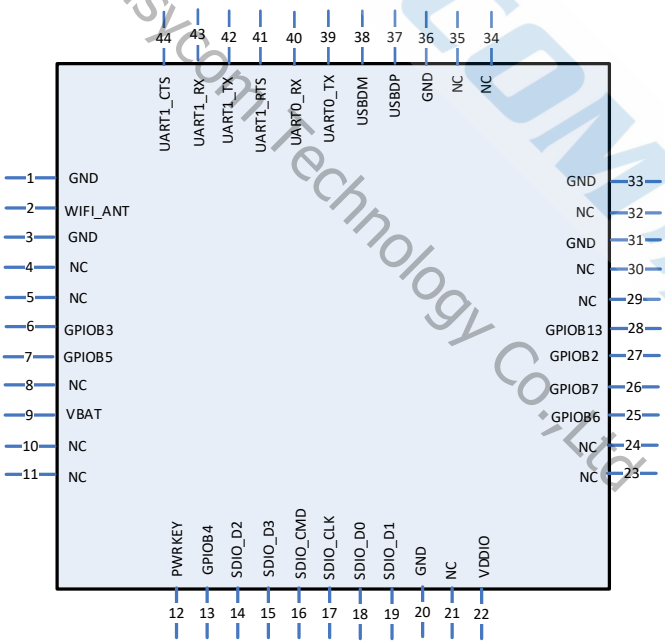


Figure 3: FSC-BW150 PIN Diagram (Top View)

3.2 PIN Definition Descriptions

Table 2: Pin definition

Pin	Pin Name	Type	Pin Descriptions	Notes
1	GND	Vss	Ground	
2	WIFI_ANT	o	WiFi 2.4G radio frequency	

			WiFi 5G radio frequency
3	GND	Vss	Ground
4	NC		
5	NC		
6	GPIOB3	I/O	General Purpose Input/ Output Pin Hang in the air when not in use, no need to connect
7	GPIOB5	I/O	General Purpose Input/ Output Pin Hang in the air when not in use, no need to connect
8	NC		
9	VBAT	PWR	3.3V Supply Voltage
10	NC		
11	NC		
12	PWRKEY	I	Module power-on pin, power-on = 1; power-off = 0; There is a 100K resistor inside the module, which is pulled up to VDD_3V3
13	GPIOB4	I/O	General Purpose Input/ Output Pin Hang in the air when not in use, no need to connect
14	SDIO_D2	I/O	SDIO Data Line 2
15	SDIO_D3	I/O	SDIO Data Line 3
16	SDIO_CMD	I/O	SDIO Command Input
17	SDIO_CLK	I	SDIO Clock Input
18	SDIO_D0	I/O	SDIO Data Line 0
19	SDIO_D1	I/O	SDIO Data Line 1
20	GND	Vss	Ground
21	NC		
22	VDDIO	PWR	1.8V~3.3V Supply Voltage
23	NC		
24	NC		
25	GPIOB6	I/O	General Purpose Input/ Output Pin Hang in the air when not in use, no need to connect
26	GPIOB7	I/O	General Purpose Input/ Output Pin Hang in the air when not in use, no need to connect
27	GPIOB2	I/O	General Purpose Input/ Output Pin Hang in the air when not in use, no need to connect
28	GPIOB13	I/O	General Purpose Input/ Output Pin
29	NC		
30	NC		
31	GND	Vss	Ground
32	NC		
33	GND	Vss	Ground
34	NC		
35	NC		
36	GND	Vss	Ground
37	USBDP	I/O	USB data D+

			Hang in the air when not in use, no need to connect
38	USDDM	I/O	USB data D- Hang in the air when not in use, no need to connect
39	UART0_TX	I/O	Debug serial port TX Hang in the air when not in use, no need to connect
40	UART0_RX	I/O	Debug serial port RX Hang in the air when not in use, no need to connect
41	UART1_RTS	O	High-Speed UART RTS
42	UART1_TX	O	High-Speed UART Data Out
43	UART1_RX	I	High-Speed UART Data In
44	UART1_CTS	I	High-Speed UART CTS

4. PHYSICAL INTERFACE

4.1 General Purpose Digital IO

The module has a total of 16 GPIO pins. By configuring the corresponding registers, these pins can be assigned different functions, including the following types of GPIO:

Only GPIO with digital function, GPIO with analog function, GPIO with capacitive touch function, etc. GPIO with analog function and GPIO with capacitive touch function can be configured as digital GPIO.

Most GPIOs with digital functions can be configured as internal pull-up/pull-down or set to high impedance. When configured as an input, the input value can be obtained by reading the register. Input pins can also be set to generate CPU interrupts by edge triggering or level triggering.

4.2 UART Interface

The four signal pins are used to implement the UART function. When FSC-BW150 is connected to another digital device, UART_RX and UART_TX transmit data between the two devices. The remaining two pins UART_CTS and UART_RTS can be used to implement RS232 hardware flow control, and both are low-level effective, that is, transmission is allowed when the level is low, and transmission is stopped when the level is high.

Table 3: Possible UART Settings

Parameter	Possible Values	
Baudrate	Minimum	110 baud (≤2%Error)
	Standard	115200bps(≤1%Error)
	Maximum	5000000bps(≤1%Error)

Flow control	RTS/CTS
Parity	None, Odd or Even
Number of stop bits	1 /2
Bits per channel	7/8

When connecting the module to a host, please make sure to follow .

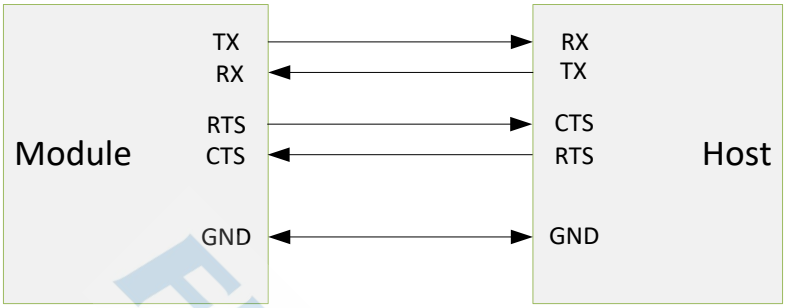


Figure 4: UART Connection

4.3 I2C Interface

I2C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I2C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

Data is transferred between a Master and a Slave synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8-bit long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to the following figure for more details about I2C Bus Timing.

- Up to two I2C bus interfaces, supporting master mode and slave mode, the frequency can be up to 400KHZ.
- 7-bit/10-bit addressing mode
- Dual addressing mode

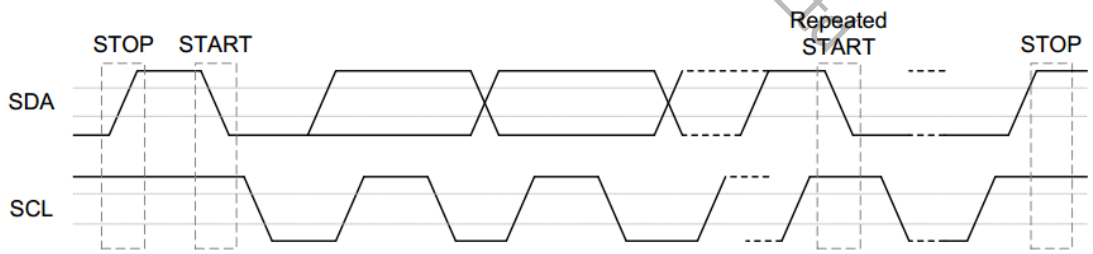


Figure 5: I2C Bus Timing

The device on-chip I2C logic provides the serial interface that meets the I2C bus standard mode specification. The I2C port handles byte transfers autonomously. The I2C H/W interfaces to the I2C bus via two pins: SDA and SCL. Pull up resistor is needed for I2C operation as these are open drain pins. When the I/O pins are used as I2C port, user must set the pins function to I2C in advance.

4.4 Analog to Digital Converter (ADC)

The device Integrated 9 channels application **14bits** ADC. The conversion range is 0V <VDDA <3.6V. The analog watchdog module can be used to detect channels that need to be kept within a specific threshold window. The configurable channel management module for analog inputs can also be used to perform conversions in single, continuous, scan, or discontinuous mode to support more advanced usage. The ADC can be triggered by events generated by an internally connected general-purpose timer (TMx) and advanced control timer (TM1). Temperature sensors can be used to generate voltages that vary linearly with temperature. Each device is factory calibrated to improve accuracy, and calibration data is stored in the system storage area.

- Conversion range: VSSA to VDDA (2.6 to 3.6V)
- Temperature Sensor

5. ELECTRICAL CHARACTERISTICS

5.1 Recommended Operating Conditions

Table 4: Recommended Operating Conditions

Parameter	Min	Type	Max	Unit
VDD_3V3	2.3	3.3	5	V
VDD_IO	1.8		3.3	°C
Operating temperature (T_A)	-20	27	+80	°C
Storage temperature (T_{stg})	-40	27	+85	°C
High-level input voltage	0.7 X VDD_IO		VDD_IO	V
Low-level input voltage	0		0.3 X VDD_IO	V

5.2 Power Consumption

Table 5: Power Consumption:

Internal Pull Resistor	Voltage	Power Consumption(mA)(Max)
VDD_3V3	3.3V	300
VDD_IO	3.3V	100
Testing Condition:	2.4GHz Tx MCS0 6.5Mbps	

FSC-BW150 Module Power Consumption:

300mA @ VDD_3V3 (Maximum) and 100mA @ VDD_IO(Maximum)

Suggest customer design power capacity are 500mA@VDD_3V3 and 200mA @ VDD_IO for FSC-BW150 Module.

6. MSL & ESD

Table 6: MSL and ESD

Parameter	Value
MSL grade:	MSL 3
ESD grade	**Electrostatic discharge**
ESD – Human-body model (HBM) rating, JESD22-A114-F (Total samples from one wafer lot)	Pass ±2000 V, all pins
ESD – Charge-device model (CDM) rating, JESD22-C101-D (Total samples from one wafer lot)	Pass ±400 V, all pins

7. RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccate (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the below and follow instructions specified by IPC/JEDEC J-STD-033.

Note: The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the below , the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccate and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60%RH.

Notice (注意) :

Feasycom module must use Step-Stencil, suggestion using the stencil thickness about 0.16-0.2mm,

it could be modify with the product.

使用我司模块，须使用阶梯钢网，建议阶梯钢网厚度0.16-0.20mm，可根据自己产品适应性，进行相应调整.

Table 6: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Feasycom surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

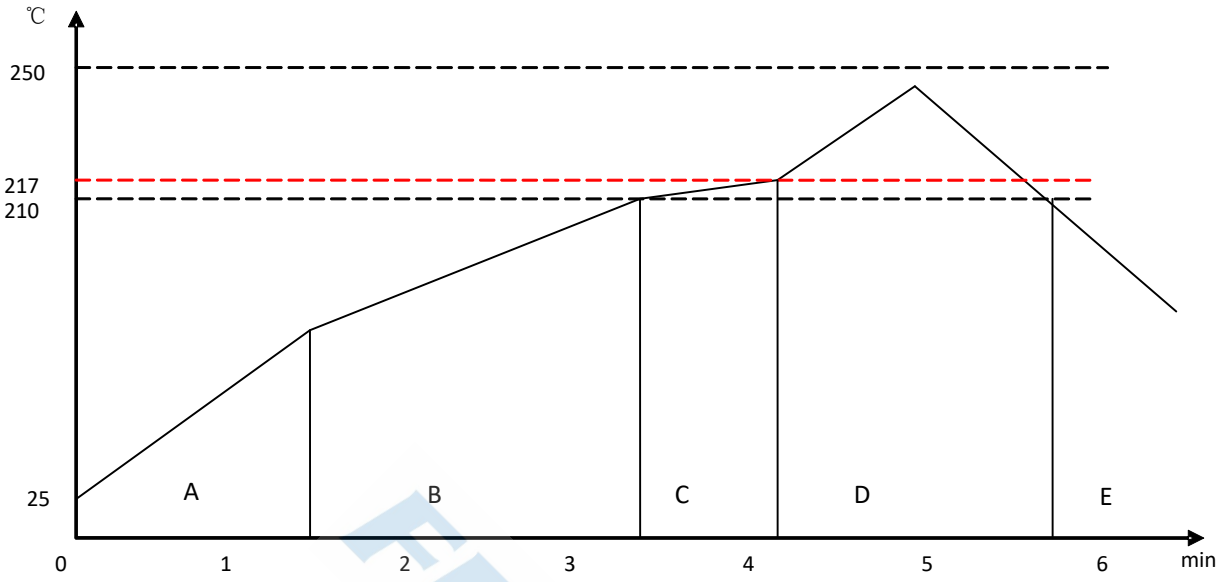


Figure 6: Typical Lead-free Re-flow

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

Equilibrium Zone 2 (C) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

8. MECHANICAL DETAILS

8.1 Mechanical Details

- Dimension: 12mm(W) x 12mm(L) x 2.2mm(H) Tolerance: ±0.2mm
- Module size: 12mm x 12mm Tolerance: ±0.2mm
- Pad size: 1.7mm x 0.5mm Tolerance: ±0.1mm
- Pad pitch: 0.9mm Tolerance: ±0.1mm

(分板后边角残留板边误差：不大于0.5mm)

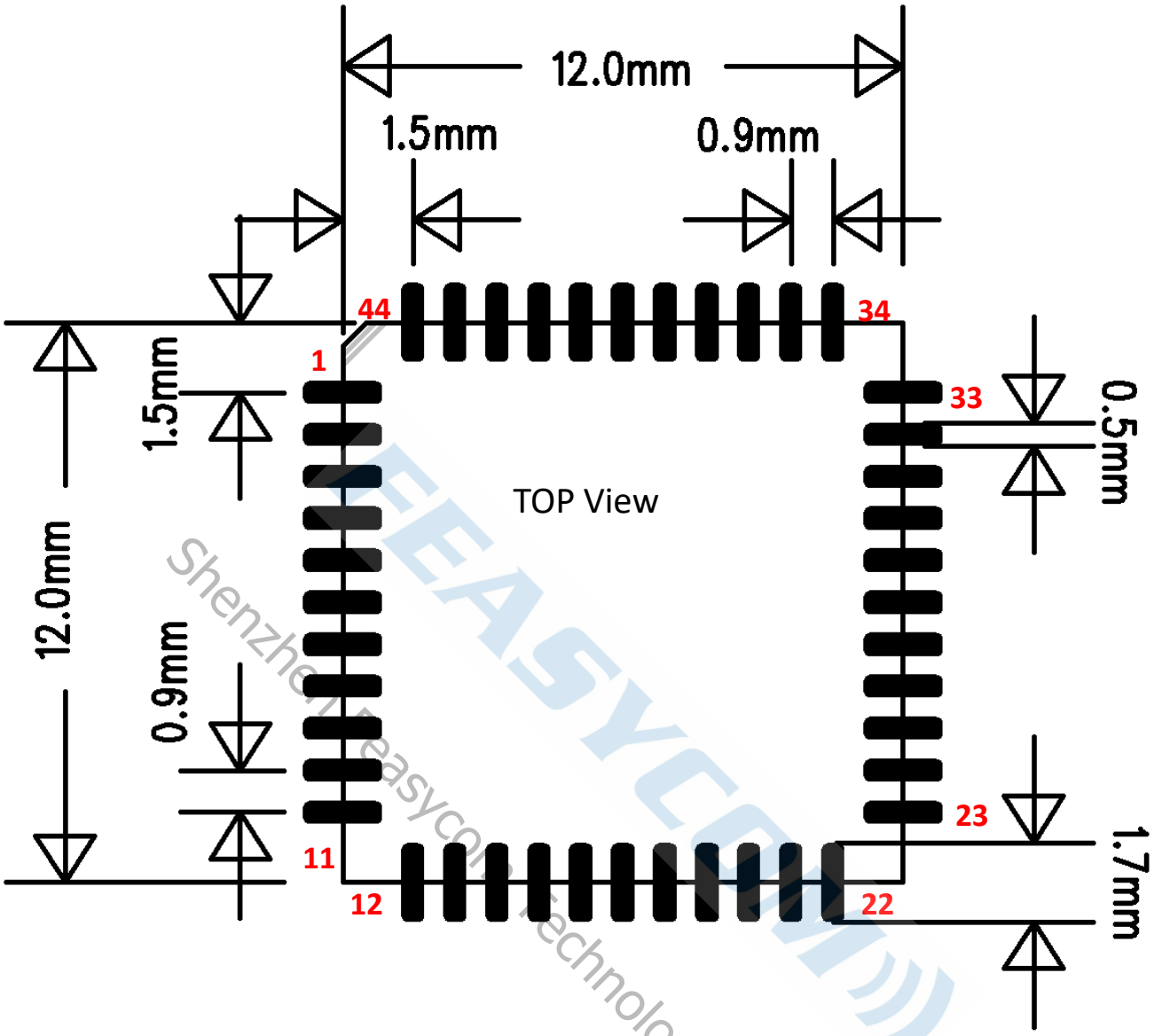


Figure 7: FSC-BW150 footprint Layout Guide (Top View)

9. HARDWARE INTEGRATION SUGGESTIONS

9.1 Soldering Recommendations

FSC-BW150 is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

9.2 Layout Guidelines(Internal Antenna)

Important Note: The antenna of FSC-BW150 needs to support both 2.4GHz and 5.8GHz dual frequency bands. We recommend using external FPC dual-band antennas instead of PCB onboard antennas. The following are general instructions for PCB onboard antennas for reference only.

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.

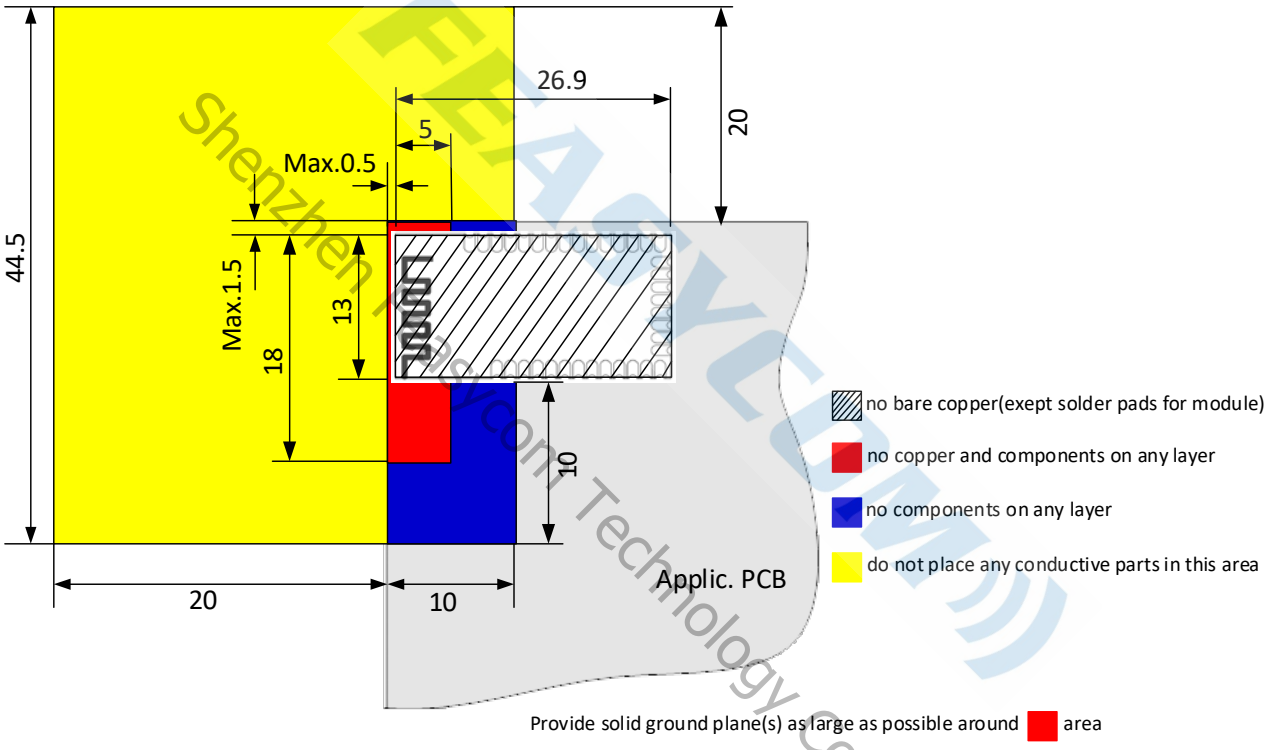


Figure 8: Restricted Area (Design schematic, for reference only. Unit: mm)

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

9.3 Layout Guidelines(External Antenna)

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The

trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

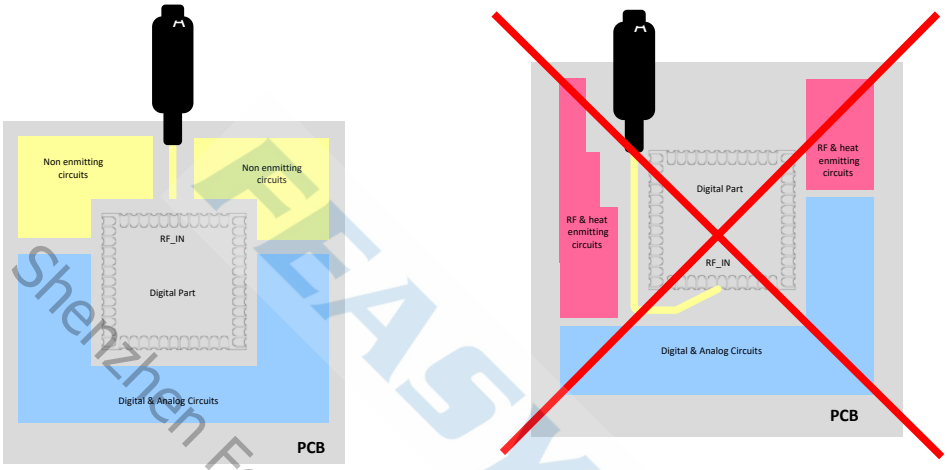


Figure 9: Placement the Module on a System Board

9.3.1 Antenna Connection and Grounding Plane Design

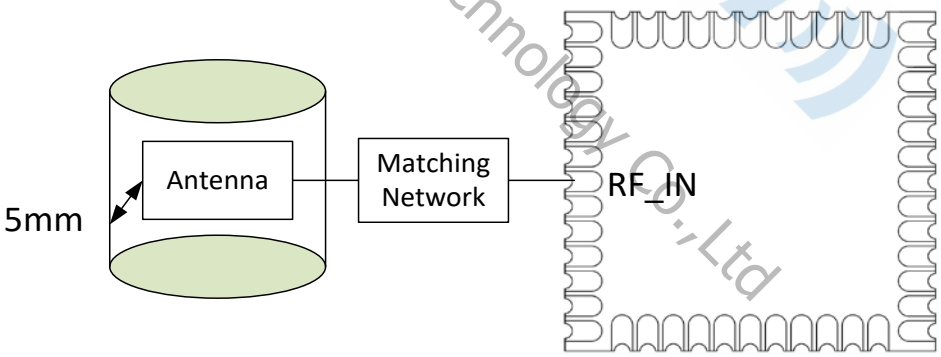


Figure 10: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

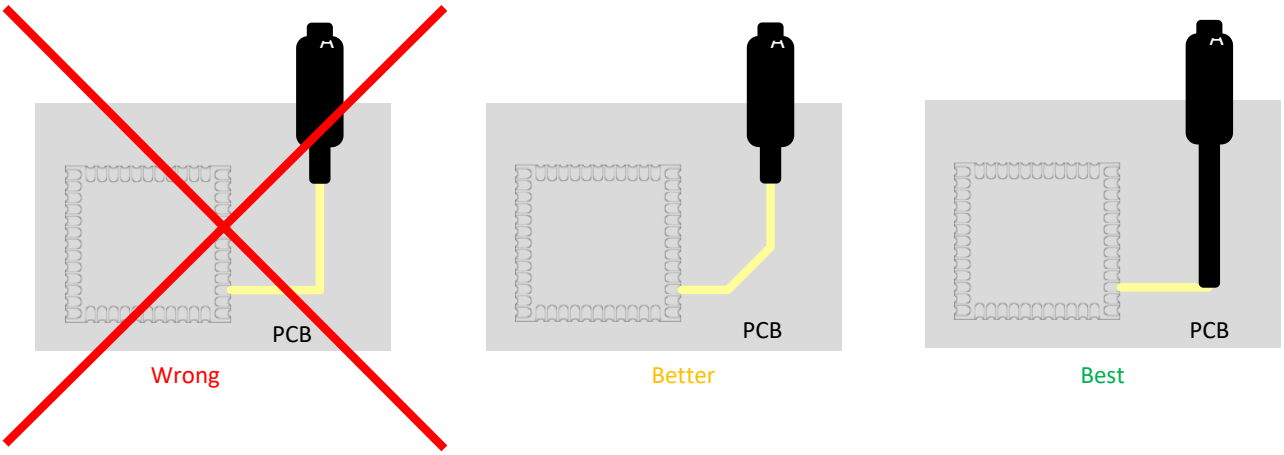


Figure 11: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

9.4 SDIO Lines Layout Guideline

The following SDIO line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive 8mA.

SDIO_DATA_CMD_WL

SDIO_DATA_CLK_WL

SDIO_DATA_0_WL ~

SDIO_DATA_3_WL

The route length of these signals be less than 15 cm and the line impedance be less than 50Ω

9.5 HCI Lines Layout Guideline

The following HCI line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive 4 ~ 8mA

UART1_RX

UART1_TX

UART1_CTS

UART1_RTS

The route length of these signals be less than 15 cm and the line impedance be less than 50Ω

9.6 Power Trace Lines Layout Guideline

VDD_3V3 Trace Width: 40mil

VDD_IO Trace Width: 20mil

9.7 Ground Lines Layout Guideline

A Complete Ground in Ground Layer.

Add Ground Through Holes to FSC-BW150 Module Ground Pads

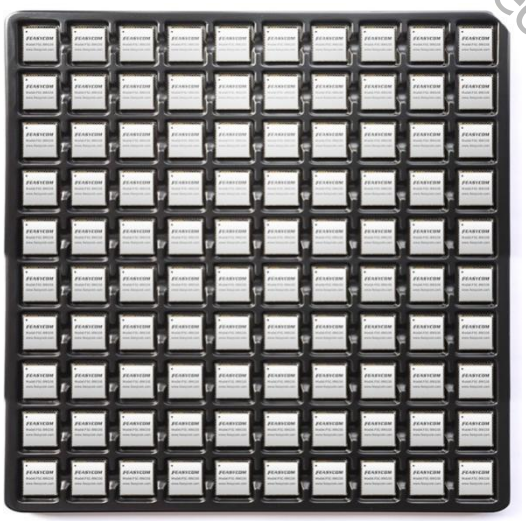
Decoupling Capacitors close to FSC-BW150 Module Power and Ground Pads

10. PRODUCT PACKAGING INFORMATION

10.1 Default Packing

a, Tray vacuum

b, Tray Dimension: 150mm * 150mm



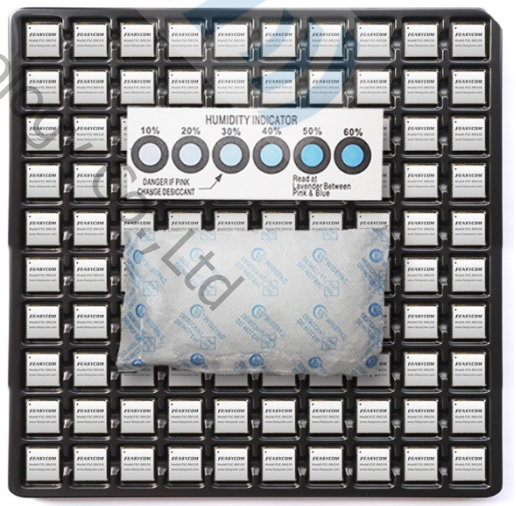


Figure 12: Tray vacuum

11. APPLICATION SCHEMATIC