FSC-BT805B

V5.2 & BR/EDR Bluetooth Module Datasheet

Version 1.3

Revision History

Version	Data	Notes	
1.0	2018/08/24	Initial Version	Devin Wan
1.1	2019/10/10	Increase the certification directory	Fish
1.2	2022/02/15	Fcorrect some description errors	Origami
1.3	2022/11/28	Update Bluetooth version to 5.2	Devin Wan

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1. INTRODUCTION

Overview

FSC-BT805B used chip is CSR8811(Bluetooth chip),it is a high performance, highly integrated multi-media bluetooth controller-chip solution with Bluetooth connectivity, which specialized in car audio applications.

Integrating all essential electronic components, including baseband, bluetooth transceiver, power management onto a single bluetooth controller chip, it offers best in class bill of material, space requirement and cost/feature ratio for bluetooth music and audio application.

With Feasycom's Bluetooth stack running on a host, designers can easily customize their applications to support different Bluetooth profiles.

FSC-BT805B is an appropriate product for designers who want to add wireless capability to their products.

Features

- Fully qualified Bluetooth v5.2 system
- Full-speed Bluetooth operation with full piconet and scatternet support
- Class 1 Bluetooth power level supported
- High-sensitivity Bluetooth receiver
- On-chip SBC encoding
- On-chip balun
- High-speed UART port (up to 4Mbps)
- 1 x PCM/I²S digital audio interfaces
- Postage stamp sized form factor
- Support External 32K OSC for standby, shutoff and sleep state (TBD)
- Support External Antenna
- RoHS compliant

Application

- Portable navigation devices
- Point of sale terminals
- Personal media players
- POS
- GPS/Car DVD

Module picture as below showing

Figure 1: FSC-BT805B Picture

2. General Specification

Table 1: General Specifications

Categories	Features	Implementation
Wireless Specification	Bluetooth chip	CSR8811
	Bluetooth Version	Dual-mode Bluetooth low energy radio Bluetooth v5.2 specification, supports BR/EDR
	Frequency	2.402 - 2.480 GHz
	Transmit Power	+9 dBm (Maximum)
	Receive Sensitivity	-95 dBm@ 0.1% BER(Typical)
	Modulation	π/4 DQPSK ,DQPSK, 8DPSK
	Raw Data Rates (Air)	2Mbps and 3Mbps EDR support
Host Interface and Peripherals	UART Interface	TX, RX,CTS,RTS
		General Purpose I/O
		Default 115200,N,8,1
		Baudrate support from 1200 to 4Mbps
		8 data bit character
	GPIO	7 (maximum – configurable) lines
	PCM/I2S	Up to 3 SCO connections
		13-bit or 16-bit linear, 8-bit u-law or A-law companded sample formats
		Receives and transmits on any selection of 3 of the first 4 slots following PCM_SYNC
Profiles	Classic Bluetooth	HFP/A2DP/AVRCP/SPP/GATT/HID/PBAP
	Bluetooth Low Energy	Support(V5.2), simultaneous BR/EDR and BLE support
Maximum Connections	Classic Bluetooth	7 Clients(TBD)
	Bluetooth Low Energy	5 Clients(TBD)
FW upgrade		No Support
Supply Voltage	Supply	2.3V~3.6V
Power Consumption		Max Peak Current(TX Power @ +9dBm TX): 70mA
Physical	Dimensions	10.8mm X 13.5mm X 2.2mm; Pad Pitch 1.0mm
Environmental	Operating	-40°C to +85°C
	Storage	-40°C to +85°C
Miscellaneous	Lead Free	Lead-free and RoHS compliant
	Warranty	One Year
Humidity		10% ~ 90% non-condensing
MSL grade:		MSL 3
ESD grade:		Human Body Model: 2000V (all pins) Machine Model: 200V (except XTAL_IN = 190V) Charged Device Model：500V (all pins)

3. HARDWARE SPECIFICATION

3.1 Block Diagram and PIN Diagram

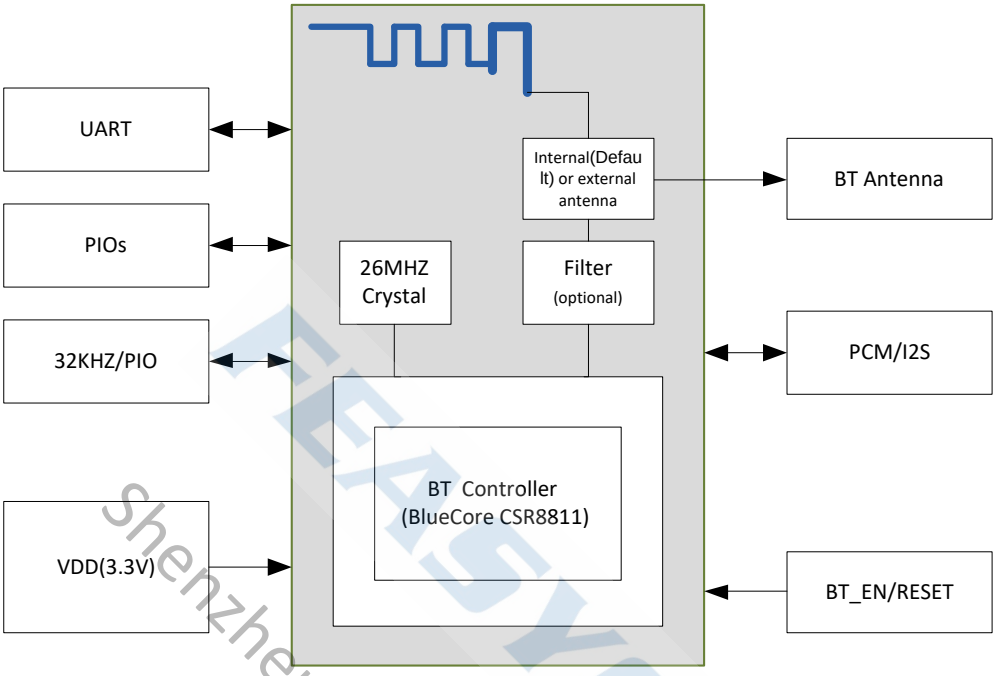


Figure 2: Block Diagram

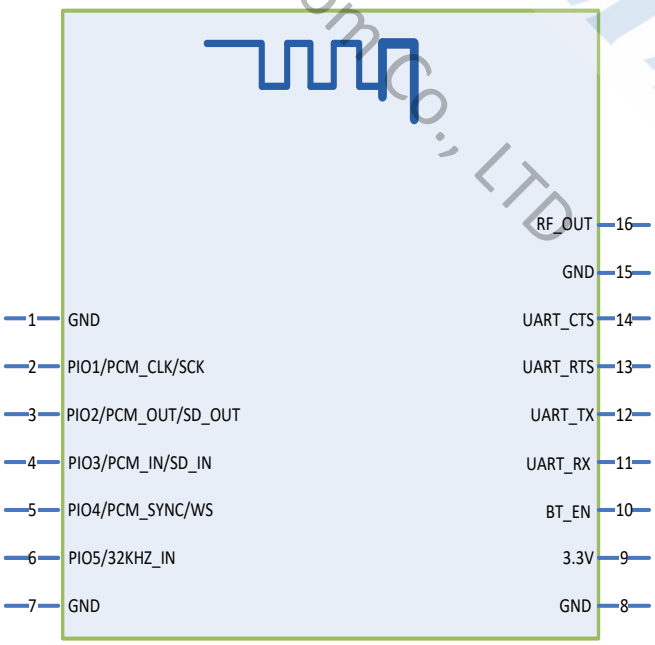


Figure 3: FSC-BT805B PIN Diagram(Top View)

3.2 PIN Definition Descriptions

Table 2: Pin definition

Pin	Pin Name	Type	Pin Descriptions	Notes
1	GND	Vss	Power Ground	
2	PIO1/PCM_CLK/SCK	I/O	Programmable input/output line Alternative Function: PCM/I2S port synchronous data clock.	Note 1
3	PIO2/PCM_OUT/SD_OUT	I/O	Programmable input/output line Alternative Function: PCM/I2S port synchronous data output.	Note 1
4	PIO3/PCM_ IN/SD_IN	I/O	Programmable input/output line Alternative Function: PCM/I2S port synchronous data input.	Note 1
5	PIO4/PCM_SYNC/WS	I/O	Programmable input/output line Alternative Function: PCM/I2S port synchronous data sync.	Note 1
6	PIO5/32KHZ_IN	I/O	Programmable input/output line Alternative Function: 32KHZ_IN	Note 2
7	GND	Vss	Power Ground	
8	GND	Vss	Power Ground	
9	3.3V	PWR	Power supply voltage 2.3V ~ 3.6V	
10	BT_EN	I	Take high to enable internal regulators.	
11	UART_RX	I/O	UART data input, active high.	Note 1
12	UART_TX	I/O	UART data output, active high.	Note 1
13	UART_RTS	I/O	UART request to send, active low.	Note 1
14	UART_CTS	I/O	UART clear to send, active low.	Note 1
15	GND	Vss	Power Ground	
16	RF_OUT	O	RF signal output .	Note 3

Module Pin Notes:

Note 1	For customized module, this pin can be work as I/O Interface.
Note 2	The sleep clock is an external 32.768kHz clock for deep sleep and other low-power modes.
Note 3	This PIN can connect to an external antenna to improve the Bluetooth signal coverage.

4. PHYSICAL INTERFACE

4.1 Power Supply

The transient response of the regulator is important. If the power rails of the module are supplied from an external voltage source, the transient response of any regulator used should be 20μs or less. It is essential that the power rail recovers quickly.

4.2 UART Interfaces

FSC-BT805B provides one channels of Universal Asynchronous Receiver/Transmitters(UART)(Full-duplex asynchronous communications). The UART Controller performs a serial-to-parallel conversion on data received from the peripheral and a parallel-to-serial conversion on data transmitted from the CPU. Each UART Controller channel supports ten types of interrupts.

This is a standard UART interface for communicating with other serial devices. The UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

When the module is connected to another digital device, UART_RX and UART_TX transfer data between the two devices.

This module output is at 3.3V CMOS logic levels (tracks VCC). Level conversion must be added to interface with an RS-232 level compliant interface.

Table 3: Possible UART Settings

Parameter	Possible Values	
Baudrate	Minimum	1200 baud (≤2%Error)
	Standard	115200bps(≤1%Error)
	Maximum	4Mbps(≤1%Error)
Flow control		RTS/CTS or none
Parity		None, Odd or Even
Number of stop bits		1/2
Bits per channel		8

When connecting the module to a host, please make sure to follow .

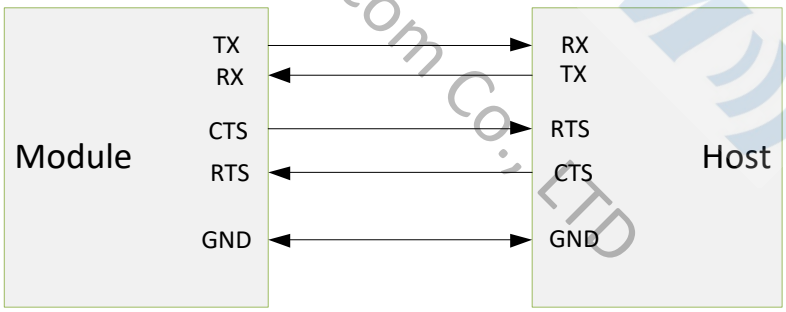


Figure 4: UART Connection

4.3 PCM Interfaces

The audio PCM interface on the FSC-BT805B supports:

- Continuous transmission and reception of PCM encoded audio data over Bluetooth.
- Processor overhead reduction through hardware support for continual transmission and reception of PCM data.
- A bidirectional digital audio interface that routes directly into the baseband layer of the firmware. It does not pass through the HCI protocol layer.

- Hardware on FSC-BT805B for sending data to and from a SCO connection.
- Up to 3 SCO connections on the PCM interface at any one time.
- PCM interface master, generating PCM_SYNC and PCM_CLK.
- PCM interface slave, accepting externally generated PCM_SYNC and PCM_CLK.
- Various clock formats including:
  - Long Frame Sync
  - Short Frame Sync
  - GCI timing environments
- 13-bit or 16-bit linear, 8-bit μ-law or A-law companded sample formats.
- Receives and transmits on any selection of 3 of the first 4 slots following PCM_SYNC.

4.3.1 PCM Interface Master/Slave

When configured as the Master of the PCM interface, FSC-BT805B generates PCM_CLK and PCM_SYNC.

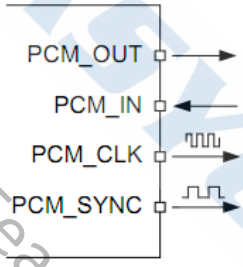


Figure 5: FSC-BT805B as PCM master

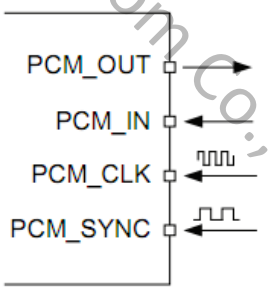


Figure 6: FSC-BT805B as PCM slave

4.3.2 Long Frame Sync

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When FSC-BT805B is configured as PCM Master, generating PCM_SYNC and PCM_CLK, then PCM_SYNC is 8-bits long. When FSC-BT805B is configured as PCM Slave, PCM_SYNC may be from two consecutive falling edges of PCM_CLK to half the PCM_SYNC rate, i.e. 62.5μs long. FSC-BT805B samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

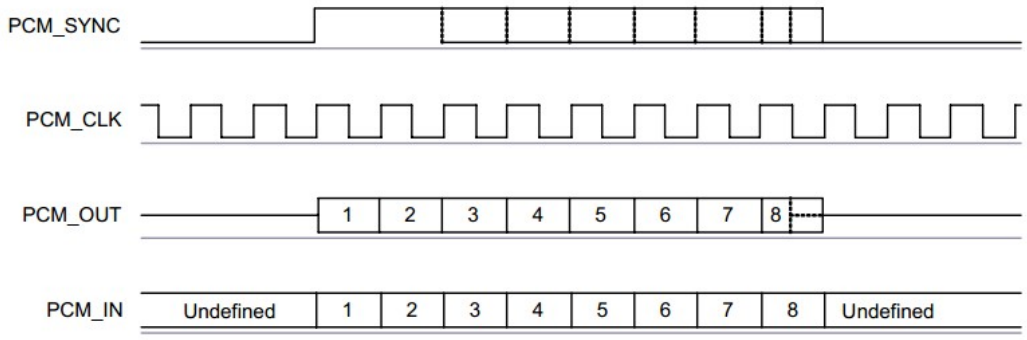


Figure 7: Long frame sync (shown with 8-bit Companded Sample)

4.3.3 Short Frame Sync

In Short Frame Sync the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always one clock cycle long.

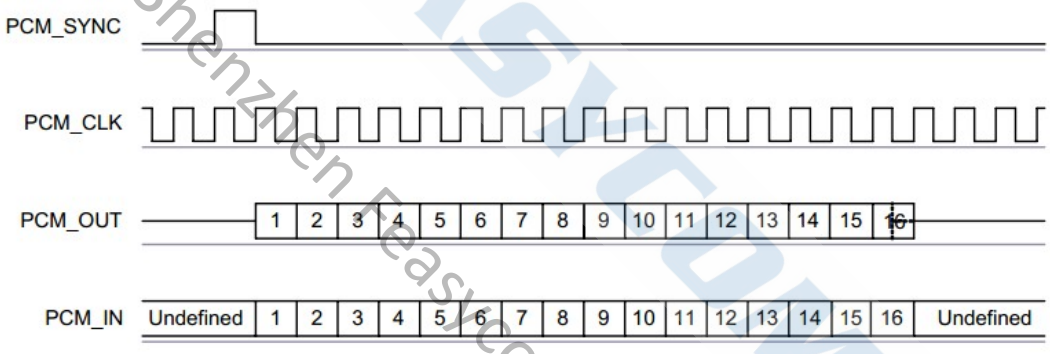


Figure 8: Short frame sync (shown with 16-bit Companded Sample)

As with Long Frame Sync, FSC-BT805B samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

4.3.4 Multi Slot Operation

More than 1 SCO connection over the PCM interface is supported using multiple slots. Up to 3 SCO connections can be carried over any of the first 4 slots.

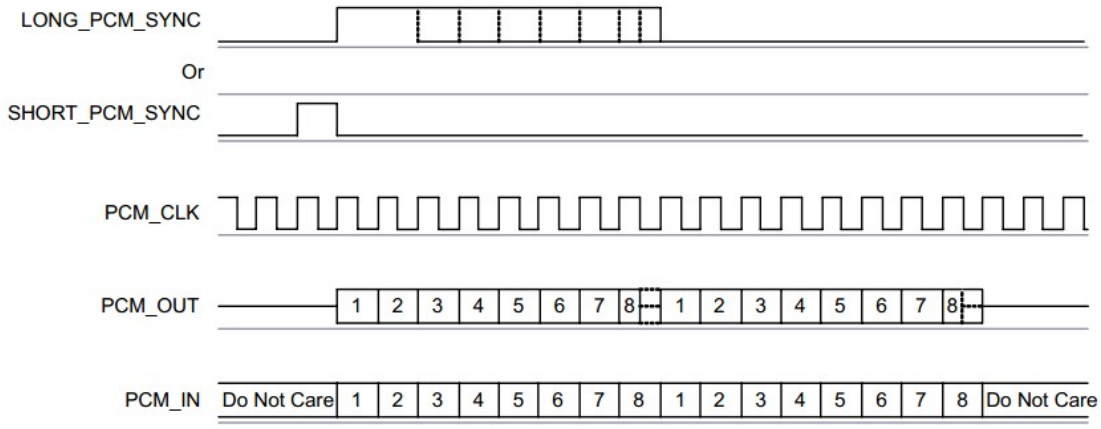


Figure 9: Multi Slot Operation with Two Slots and 8-bit Companded Samples

4.3.5 GCI Interface

FSC-BT805B is compatible with the General Circuit Interface, a standard synchronous 2B+D ISDN timing interface. The two 64Kbps B channels can be accessed when this mode is configured.

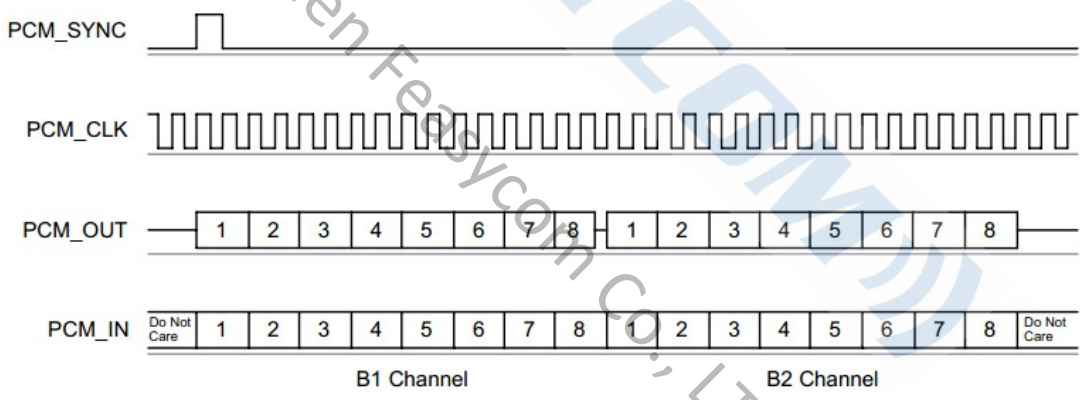


Figure 10: GCI Interface

The start of frame is indicated by the rising edge of PCM_SYNC and runs at 8K Hz.

4.3.6 Slots and Sample Formats

FSC-BT805B receives and transmits on any selection of the first 4 slots following each sync pulse. Slot durations are either 8 or 16 clock cycles:

- 8 clock cycles for 8-bit sample formats.
- 16 clock cycles for 8-bit, 13-bit or 16-bit sample formats.

FSC-BT805B supports:

- 13-bit linear, 16-bit linear and 8-bit u-law or A-law sample formats.

- A sample rate of 8ksps.
- Little or big endian bit order.
- For 16-bit slots, the 3 or 8 unused bits in each slot are filled with sign extension, padded with zeros or a programmable 3-bit audio attenuation compatible with some codecs.

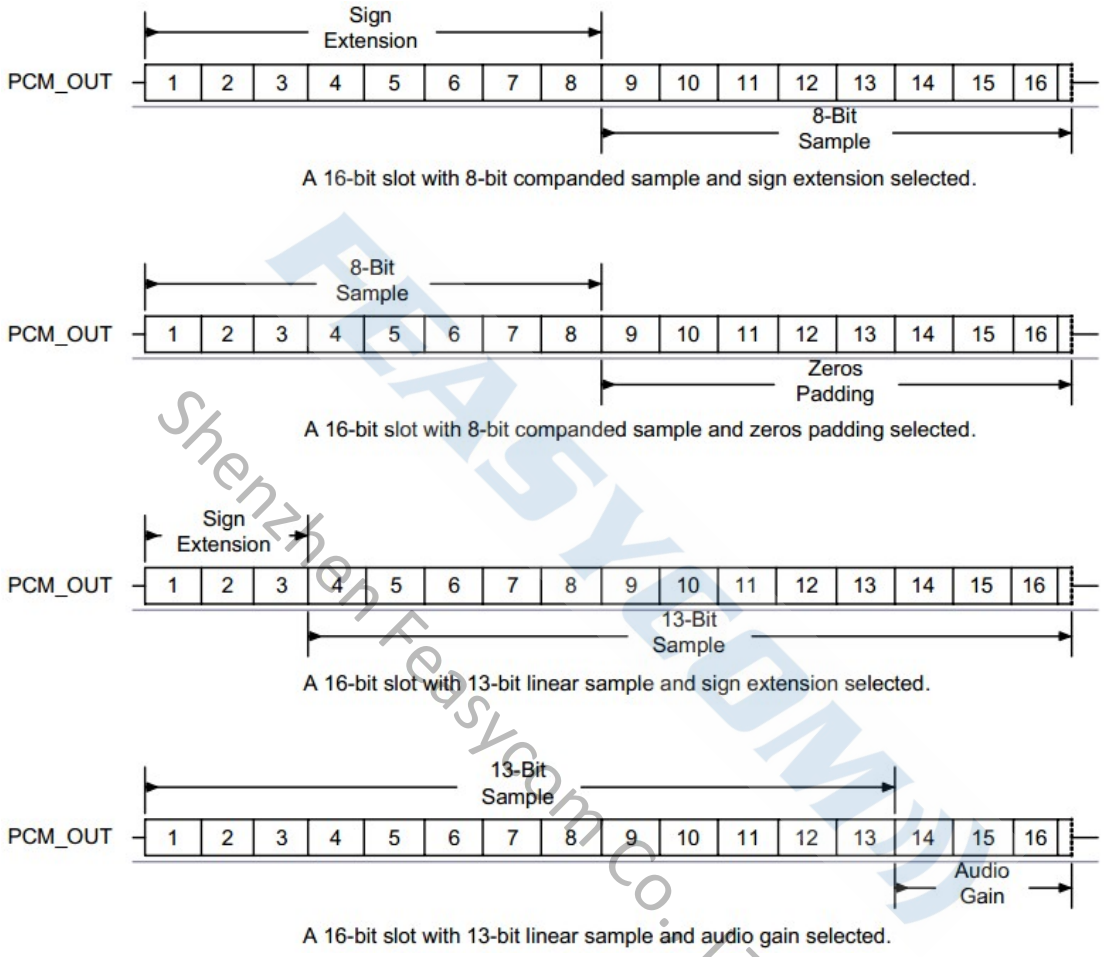


Figure 11: 16-bit slot length and sample formats

4.3.7 Additional Features

FSC-BT805B has a mute facility that forces PCM_OUT to be 0. In Master mode, PCM_SYNC may also be forced to 0 while keeping PCM_CLK running which some CODECS use to control power down.

4.4 Digital Audio Interface (I²S)

The digital audio interface supports the industry standard formats for I2S, left-justified or right-justified. The interface shares the same pins as the PCM interface, which means each audio bus is mutually exclusive in its usage.

The internal representation of audio samples within BlueCore6-ROM QFN is 16-bit and data on SD_OUT is limited to 16-bit per channel.

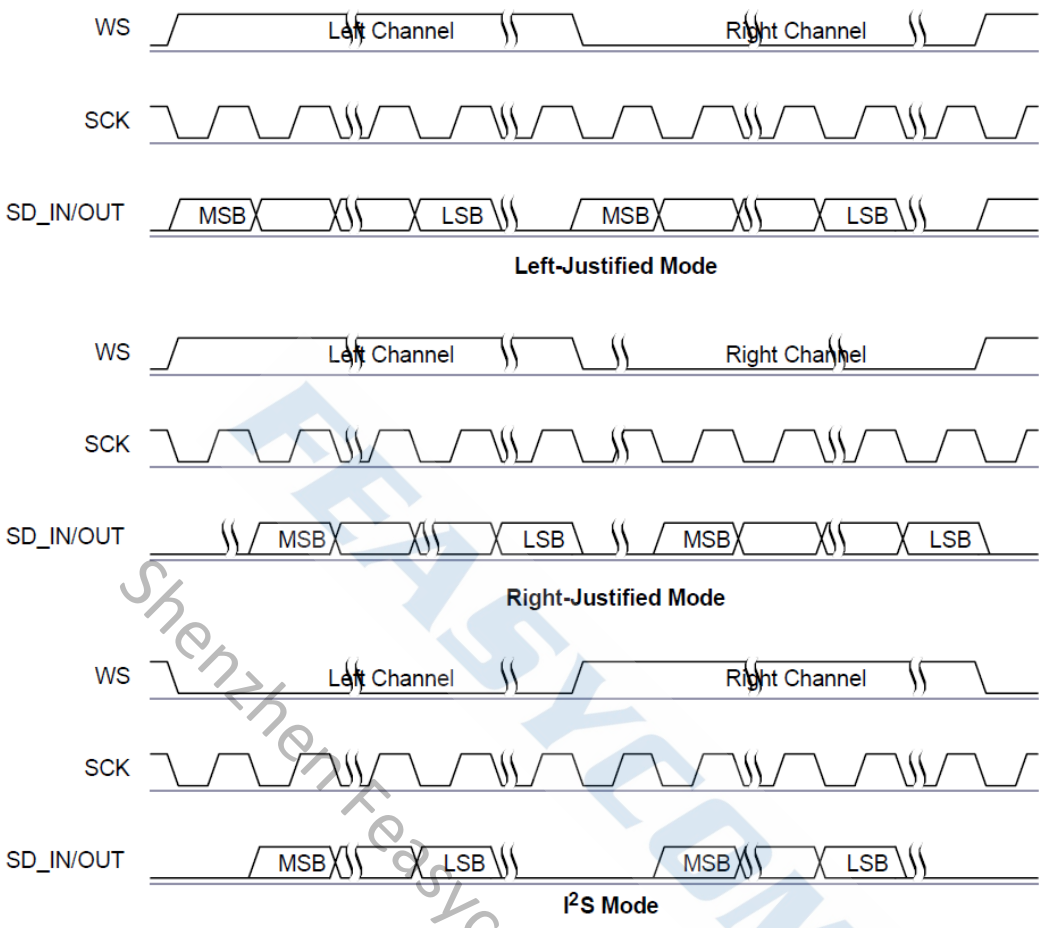


Figure 12: Digital Audio Interface Modes

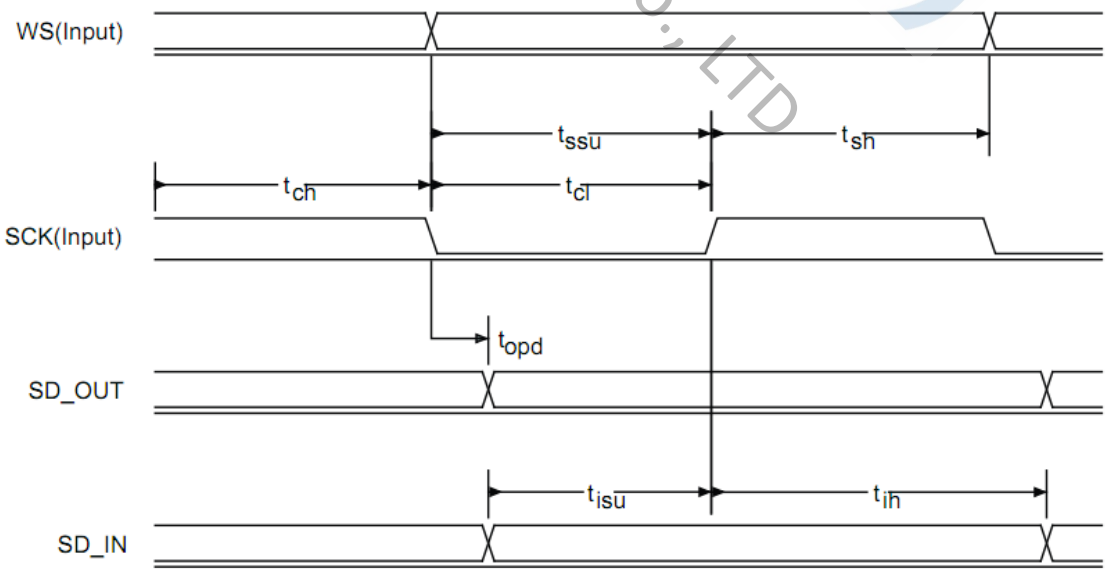


Figure 13: Digital Audio Interface Slave Timing

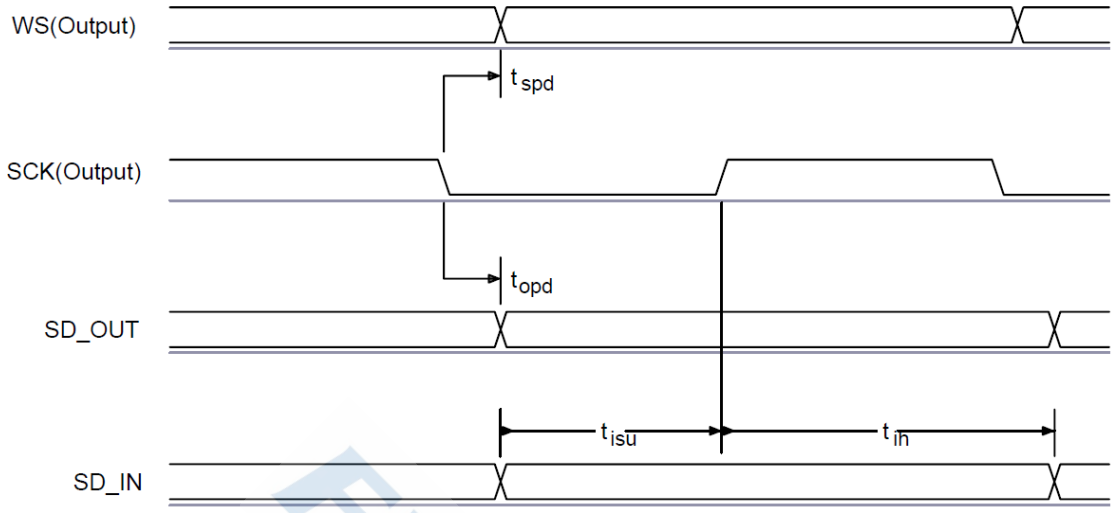


Figure 14: Digital Audio Interface Master Timing

4.5 Reset

The module is reset from several sources:

- BT_EN Pin
- Power-On Reset
- A UART break character
- Via a software-configured watchdog timer

The BT_EN pin is an active low reset. To ensure a full reset the reset signal must be asserted for a period greater than 5ms.

A warm reset function is also available under software control. After a warm reset the RAM data remains available.

The VREG_EN_RST# pin is pulled down internally until the VDD_DIG rail is turned on. Then the pull switches to a strong pull-up.

4.6 General Purpose Digital IO

There are 7 general purpose digital IOs defined in the module.

The PIO lines are configured in software to have either weak or strong pull-ups or pull-downs. All PIO lines are configured as inputs with weak pull-downs at reset.

4.7 RF Interface

For This Module, the default mode for antenna is external antenna.

The user can connect a 50 ohm antenna directly to the RF port.

- 2402–2480MHz Bluetooth 5.2; 2 Mbps to 3 Mbps over the air data rate.
- TX output power of +9dBm.
- Receiver to achieve maximum sensitivity -95dBm @ 0.1% BER.

5. ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

Absolute maximum ratings for supply voltage and voltages on digital and analogue pins of the module are listed below. Exceeding these values causes permanent damage.

The average PIO pin output current is defined as the average current value flowing through any one of the corresponding pins for a 100mS period. The total average PIO pin output current is defined as the average current value flowing through all of the corresponding pins for a 100mS period. The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

Table 4: Absolute Maximum Rating

Parameter	Min	Max	Unit
Storage temperature	-40	+85	°C
VDD(3.3V)	-0.4	+3.6	V
I/O supply voltage	-0.4	+3.6	V
Other terminal voltages	VSS - 0.4V	VDD(3.3V)+0.4V	V

5.2 Recommended Operating Conditions

Table 5: Recommended Operating Conditions

Parameter	Min	Type	Max	Unit
Operating temperature	-40	+25	+85	°C
VDD(3.3V)	2.3	3.3	3.6	V
I/O supply voltage	2.3	3.3	3.6	V

5.3 Input/output Terminal Characteristics(UART,PCM/I2S,I/O)

Table 6: DC Characteristics (V_{DD} - V_{SS} = 3.3V, T_A = 25°C)

Parameter	Min	Type	Max	Unit
Input Voltage				

V_{IL} -	Input Low Voltage	-0.4	-	0.4	V
V_{IH} -	Input High Voltage	0.7XVDD	-	VDD+0.4	V
	Tr/Tf	-	-	25	nS
Output Voltage					
V_{OL} -	Low Level Output Voltage, I_{OL} = 4.0mA	-	-	0.4	V
V_{OH} -	High Level Output Voltage, I_{OH} = -4.0mA	0.75XVDD	-	-	V
	Tr/Tf	-	-	5	nS
Input and Trlstate Currents					
Strong pull-up		-150	-40	-10	uA
Strong pull-down		10	40	150	uA
Weak pull-up		-5	-1.0	-0.33	uA
Weak pull-down		0.33	1.0	5.0	uA
C_I Input Capacitance		1.0	-	5.0	pF

5.4 Specifications of Power-on Reset

Table 7: Specifications of Power-on Reset

Parameter	Min	Type	Max	Unit
Reset release on VDD_DIG rising (HI)	1.05	-	1.15	°V
Reset assert on VDD_DIG falling (awake)	HI - 0.060	-	HI - 0.045	V
Reset assert on VDD_DIG falling (deep sleep)	0.80	0.825	0.86	V

5.5 External Sleep Clock Specification

Table 8: Sleep Clock Specification

Sleep Clock			Min	Type	Max	Unit
Frequency[a]			30	32.768	35	KHz
Frequency tolerance[b]			-	-	250	±ppm
Duty cycle			30:70	50:50	70:30	%
Jitter Integrated rms jitter 10Hz to 20kHz		f_{ref} = 32.768kHz	-	-	20	ns rms
Phase noise	fref = 32.768kHz	1kHz offset	-	-	-100	dBc/Hz
Phase noise	fref = 32.768kHz	10kHz offset	-	-	-120	dBc/Hz

(a) Stability is most important as frequency is calibrated against the system clock.
(b) The frequency of the slow clock is periodically calibrated against the system clock, as a result the rate of change of the frequency is more important than the maximum deviation.

5.6 Power consumptions(TBD)

Table 9: Power consumptions

Operation	Connection Type	Average	Unit
Page scan, time interval 1.28s	-	0.4	mA
Inquiry and page scan, time interval 1.28s	-	0.8	mA
ACL no traffic	Master	4	mA
ACL with file transfer	Master	9	mA
ACL 40ms sniff	Master	2	mA
ACL 1.28s sniff	Master	0.2	mA
eSCO EV5	Master	12	mA
eSCO EV3	Master	18	mA
eSCO EV3 – hands-free –setting S1	Master	18.5	mA
SCO HV1	Master	37	mA
SCO HV3	Master	17	mA
SCO HV3 30ms sniff	Master	17	mA
ACL no traffic	Slave	14	mA
ACL with file tranfer	Slave	17	mA
ACL 40ms sniff	Slave	1.6	mA
ACL 1.28s sniff	Slave	0.2	mA
eSCO EV5	Slave	19	mA
eSCO EV3	Slave	23	mA
eSCO EV3 - hands-free - setting S1	Slave	23	mA
SCO HV1	Slave	37	mA
SCO HV3	Slave	23	mA
SCO HV3 30ms sniff	Slave	16	mA
Standby host connection (Deep-Sleep)	-	40	mA
Reset (active low)	-	39	mA

6. MSL & ESD

Table 10: MSL and ESD

Parameter	Value
MSL grade:	MSL 3
ESD grade:	(Human Body Model Contact Discharge per JEDEC EIA/JESD22-A114) ESD_HAND_HBM -> 2000V (all pins)
	(Machine Model Contact Discharge per JEDEC EIA/JESD22-A115) ESD_HAND_MM -> 200V (except XTAL_IN = 190V)
	(Charged Device Model Contact Discharge per JEDEC EIA/JESD22-C101) ESD_HAND_CDM -> 500V (all pins)

7. RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccate (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the below next table and follow instructions specified by IPC/JEDEC J-STD-033.

Note: The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the below next table, the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccate and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60%RH.

Table 11: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Feasycom surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

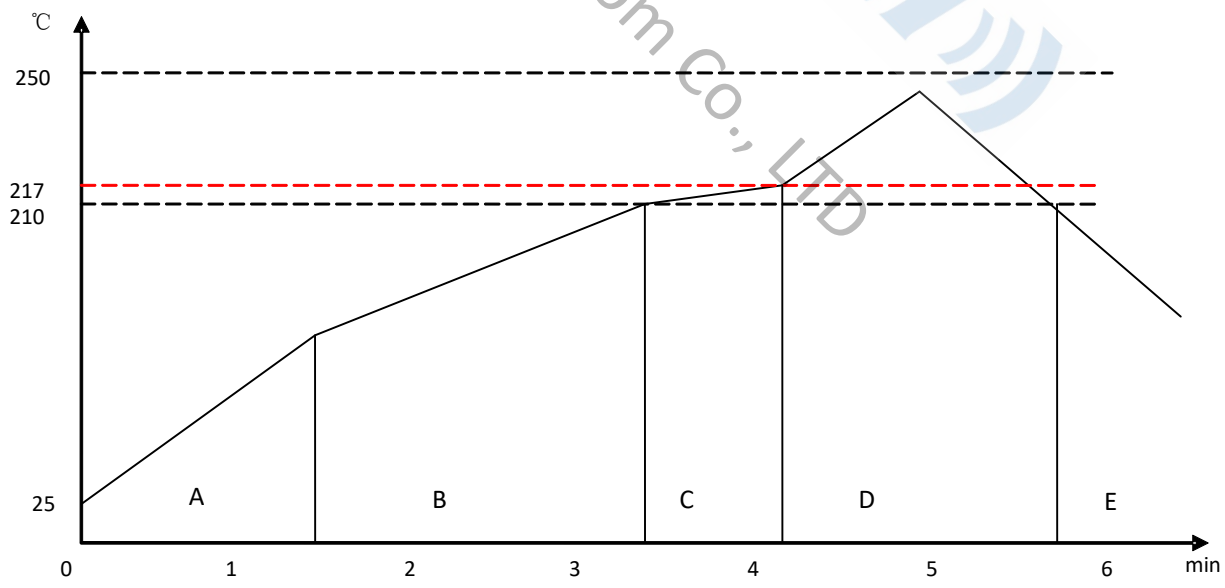


Figure 15: Typical Lead-free Re-flow

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

Equilibrium Zone 2 (C) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

8. MECHANICAL DETAILS

8.1 Mechanical Details

- Dimension: 10.8mm(W) x 13.5mm(L) x 2.2mm(H) Tolerance: ±0.2mm
- Module size: 10.8mm X 13.5mm Tolerance: ±0.2mm
- Pad size: 2.0mmX0.6mm Tolerance: ±0.1mm
- Pad pitch: 1.0mm Tolerance: ±0.1mm

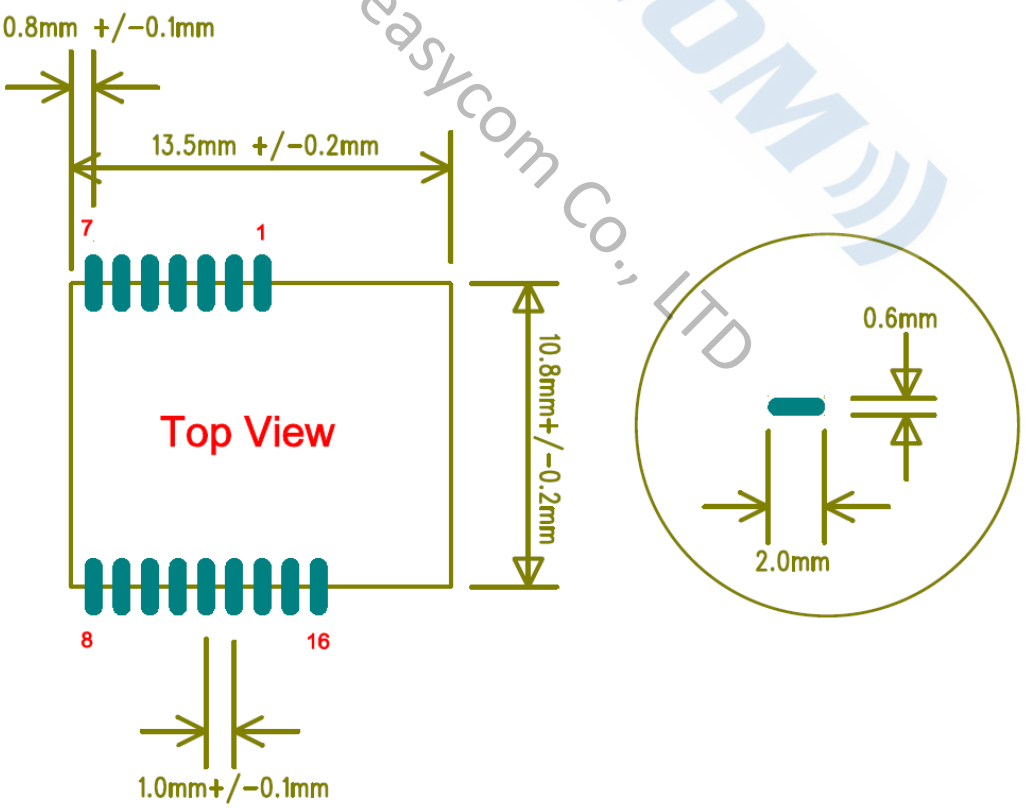


Figure 16: FSC-BT805B footprint

9. HARDWARE INTEGRATION SUGGESTIONS

9.1 Soldering Recommendations

FSC-BT805B is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

9.2 Layout Guidelines(Internal Antenna)

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.

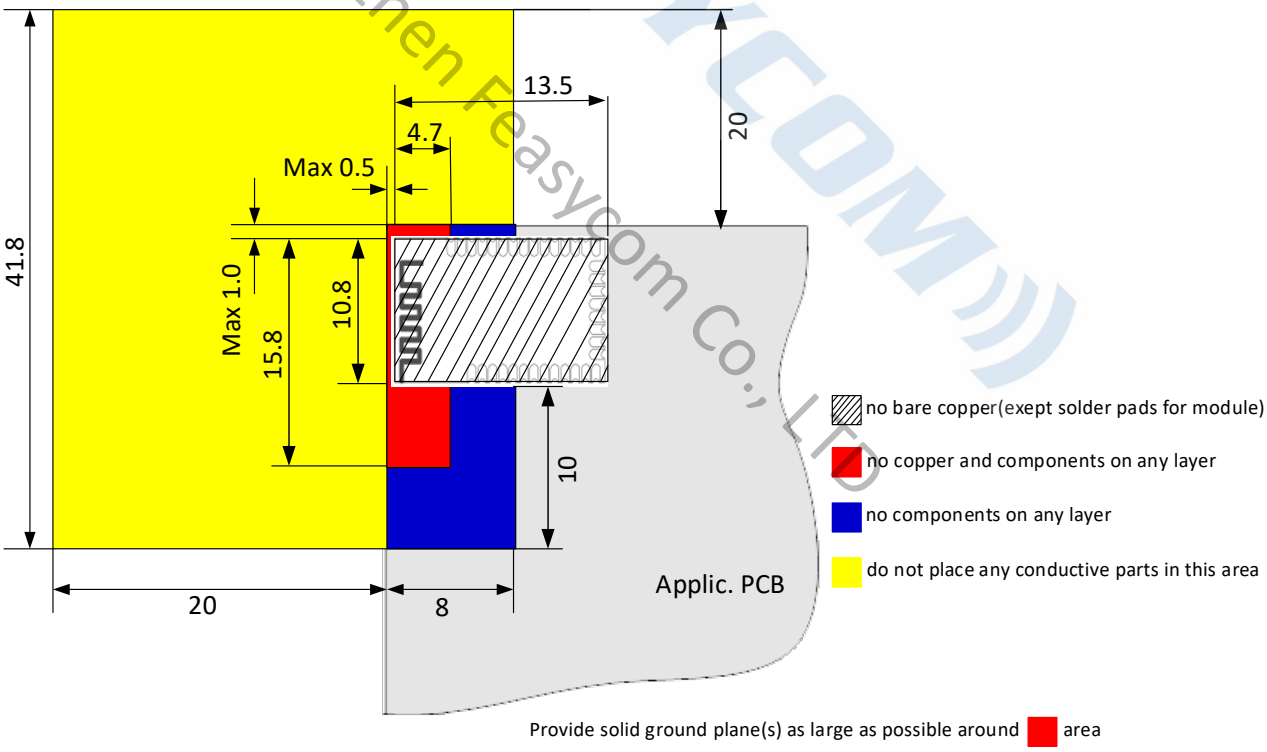


Figure 17: FSC-BT805B Restricted Area （Unit: mm）

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive

signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

9.3 Layout Guidelines(External Antenna)

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

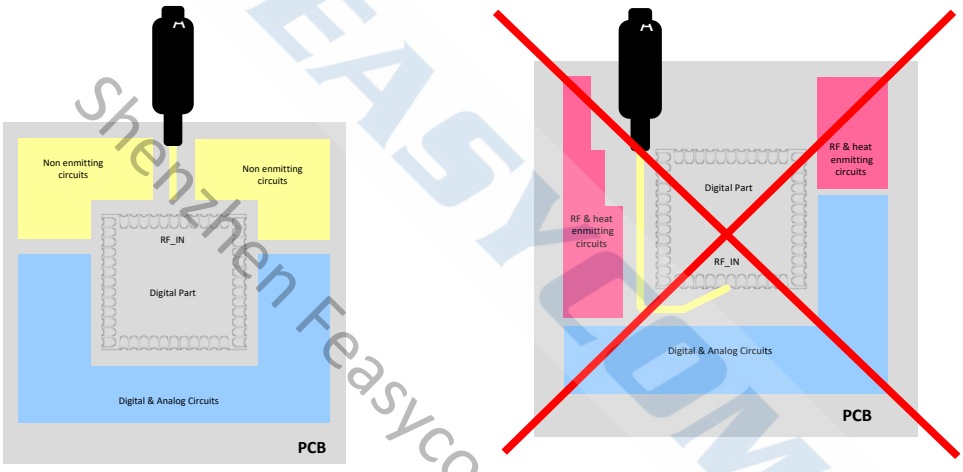


Figure 18: Placement the Module on a System Board

9.3.1 Antenna Connection and Grounding Plane Design

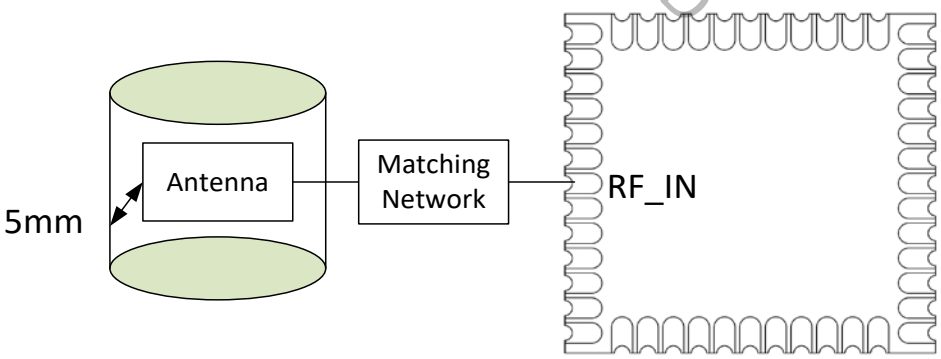


Figure 19: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.

- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

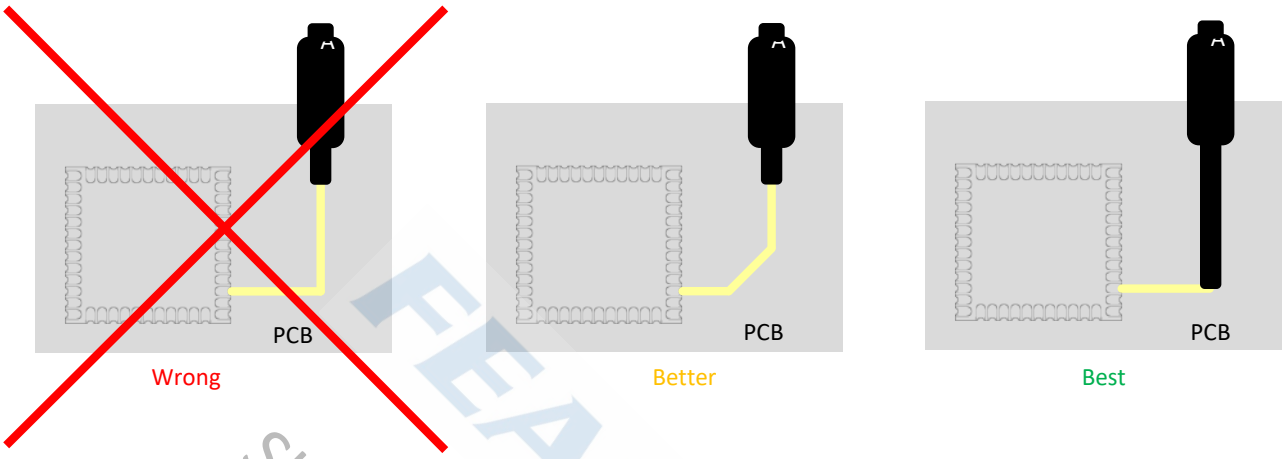


Figure 20: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

10. PRODUCT PACKAGING INFORMATION

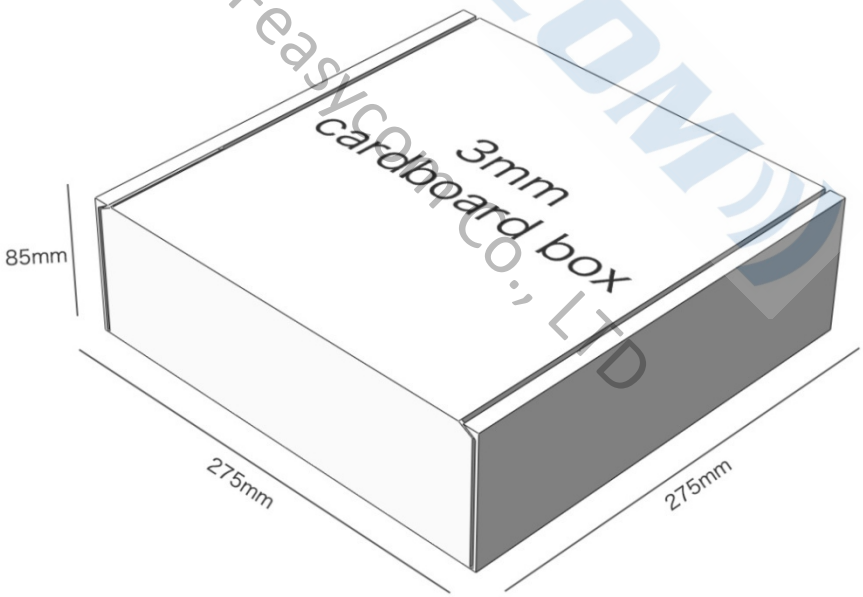
10.1 Default Packing

a, Tray vacuum

b, Tray Dimension: 180mm * 195mm

Figure 21: Tray vacuum

10.2 Packing box(Optional)



* If require any other packing, must be confirmed with customer

* Package: 1000PCS Per Carton (Min Carton Package)

Figure 22: Packing Box

11. CERTIFICATION

11.1 Certificate Picture

Has passed SRRC certification.

无线电发射设备
Radio Transmission Equipment
型号核准证
Type Approval Certificate

深圳市飞易通科技有限公司：

根据《中华人民共和国无线电管理
In accordance with the provisions on the Radio
条例》，经审查，下列无线电发射设备
Regulations of the People's Republic of China , the following
符合中华人民共和国无线电管理规定和
radio transmission equipment , after examination , conforms
技术标准，其核准代码为：CMIIT ID: 2019DP8741
to the provisions with its CMIIT ID:

有效期：五年
Validity

（发证机关）
Sealed by issuing authority
2019年 9 月 11日
Year Month Date

编号：2019-8741
Number

设备名称：蓝牙模块
Equipment Name

设备型号：FSC-BT805B
Equipment Type

主要功能：数据传输
Main Functions

调制方式：GFSK π/4-DQPSK 8DPSK
Modulation Mode

主要技术参数及其指标值：
Main Technical Parameters

频率范围：2400-2483.5MHz
Frequency Range

频率容限：≤20ppm
Frequency Tolerance

发射功率：≤20dBm(EIRP)
Transmitting Power

占用带宽：≤2MHz
Occupied Bandwidth

杂散发射限值：≤-30dBm
Spurious Emission Limits

（核发单位章）
Sealed by issuing authority
2019年 9 月 11日
Year Month Date

12. APPLICATION SCHEMATIC