FSC-BT660

DATASHEET V1.0

1 INTRODUCTION

Overview

FSC-BT660 are ideal for mesh IoT wireless connectivity using Matter, OpenThread.

By default, FSC-BT660 module is equipped with powerful and easy-to-use Feasycom firmware. It's easy t o use and completely encapsulated. Feasycom firmware enables users to access wireless functionality wit h simple ASCII commands delivered to the module over serial interface - it's just like a wireless modem.

Therefore, FSC-BT660 provides an ideal solution for developers who want to integrate wireless technology into their design.

Features

- **Low Power Wireless System**
  - High Performance 32-bit 78 MHz ARM Cortex®-M33 with DSP instruction and floating-point unit for efficient signal processing
  - 2.4 GHz radio operation
  - Matrix Vector Processor for AI/ML acceleration
- **Radio Performance**
  - -105.4 dBm sensitivity @ 250 kbps O-QPSK DSSS
  - -105.7 dBm sensitivity @ 125 kbps GFSK
  - -97.6 dBm sensitivity @ 1 Mbps GFSK
  - -94.8 dBm sensitivity @ 2 Mbps GFSK
  - TX power up to 19.5 dBm
- **Low System Energy Consumption:**
  - 4.4 mA RX current (1 Mbps GFSK)
  - 5.1 mA RX current (250 kbps O-QPSK DSSS)
  - 5 mA TX current @ 0 dBm output power
  - 19.1 mA TX current @ 10 dBm output power
  - 156.8 mA TX current @ 19.5 dBm output power
  - 33.4 µA/MHz in Active Mode (EM0) at 39.0 MHz
  - 1.3 µA EM2 DeepSleep current (16 kB RAM retention and RTC running from LFRCO)
- **Wide selection of module peripherals:**
  - Analog to Digital Converter (IADC)
  - 12-bit @ 1 Msps or 16-bit @ 76.9 ksps

• Select OPNs support High Speed Mode (up to 2 Msps) and High Accuracy Mode (up to 16 bits ENOB at 3.8 ksps)
• 2 × Analog Comparator (ACMP)
• 2 × Digital to Analog Converter (VDAC)
• Up to 32 General Purpose I/O pins with output state retention and asynchronous interrupts
• 3 × 16-bit Timer/Counter with 3 Compare/Capture/PWM channels (TIMER2/3/4)
• 2 × 32-bit Timer/Counter with 3 Compare/Capture/PWM channels (TIMER0/1)
• 1 × Universal Synchronous/Asynchronous Receiver/Transmitter (USART), supporting UART/SPI/SmartCard (ISO 7816)/IrDA/I2S
• 2 × Enhanced Universal Synchronous/Asynchronous Receiver/ Transmitter (EUSART) supporting UART/SPI/DALI/ IrDA
• 2 × I2C interface with SMBus support
• Low-Frequency RC Oscillator with precision mode to replace 32 kHz sleep crystal (LFRCO)
• Keypad scanner supporting up to 6x8 matrix (KEYSCAN)
• Die temperature sensor with +/-1.5 °C accuracy after singlepoint calibration

➢ **Protocol Support**:

• Matter
• OpenThread
• Bluetooth Low Energy (BLE 5.3)
• Bluetooth Mesh
• Proprietary 2.4 GHz
• Multiprotocol

➢ **Application**:

- Smart Home - Gateways and hubs, sensors, switches, door locks, smart plugs
- Lighting - LED bulbs, luminaires
- Building Automation - Gateways, sensors, switches, location services
- AI/ML - Predictive maintenance, glass break detection, wake-word detection

2 General Specification

Table 2-1：General Specifications

Categories	Features	Implementation
2.4 GHz radio	Transmit Power	+19.5 dBm（max）
Interface		UART/I²C/SPI
Size		12mm × 15 mm × 1.7mm
Operating temperature		-40°C ~+125°C
Storage temperature		-40°C ~+85°C
Supply Voltage		1.71V~3.8V
Miscellaneous	Lead Free Warranty	Lead-free and RoHS compliant One Year
Humidity		10% ~ 90% non-condensing
MSL grade:		MSL 3
ESD grade:		Human Body Model: Pass ±2000 V, Charge device model: Pass ±500 V,

3 HARDWARE SPECIFICATION

3.1 Block Diagram and PIN Diagram

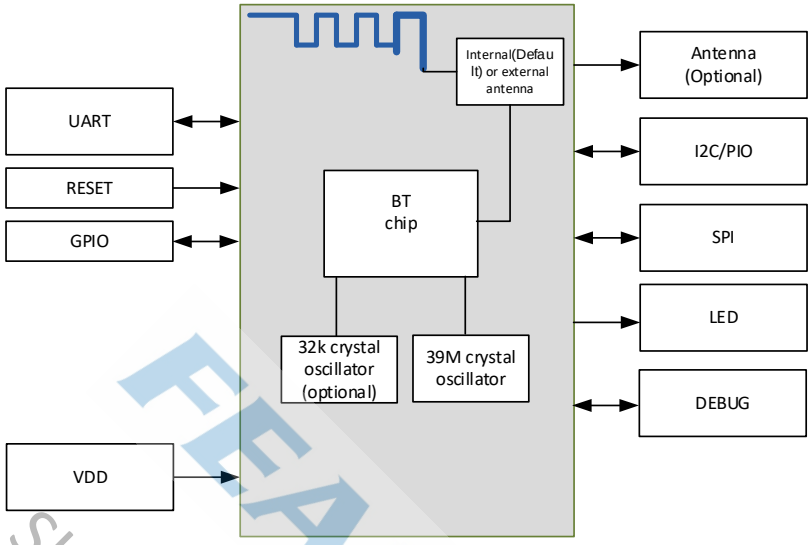

Figure 3-1:Block Diagram

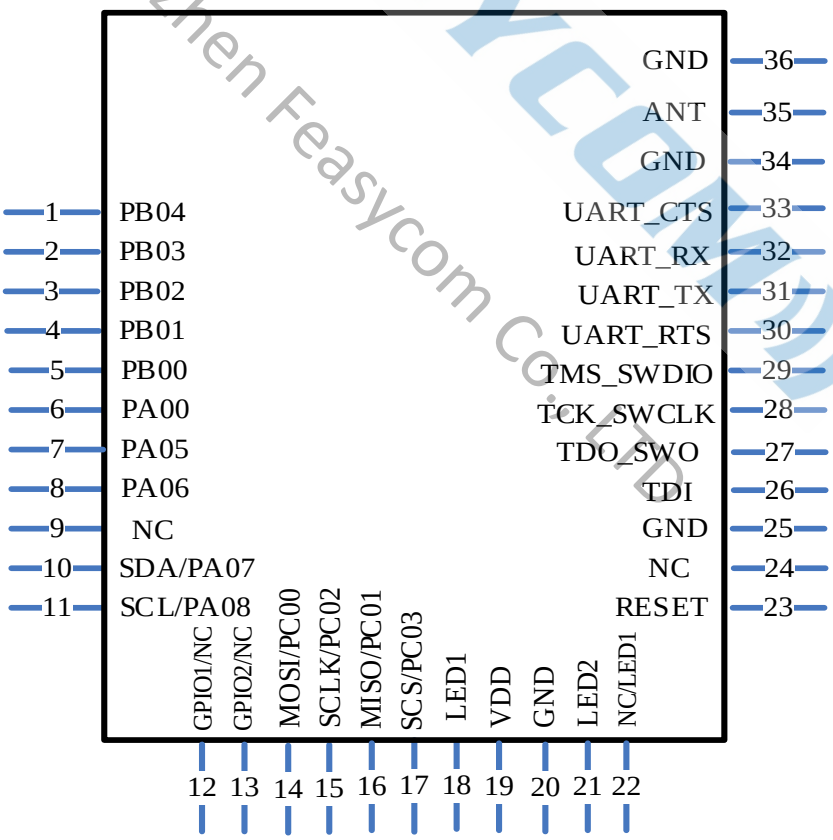

Figure 3-2:FSC-BT660 PIN Diagram(Top View)

3.2 PIN Definition Descriptions

Table 3-2： Pin definition

Pin	Pin Name	Type	Pin Descriptions	Notes
1	PB04	I/O	Programmable I/O	
2	PB03	I/O	Programmable I/O	
3	PB02	I/O	Programmable I/O	
4	PB01	I/O	Programmable I/O	
5	PB00	I/O	Programmable I/O	
6	PA00	I/O	Programmable I/O	
7	PA05	I/O	Programmable I/O	
8	PA06	I/O	Programmable I/O	
9	NC	-	NC	
10	SDA/PA07	I/O	Programmable I/O Alternative function : I2C_SDA	
11	SCL/PA08	I/O	Programmable I/O Alternative function : I2C_SCL	
12	GPIO1/NC	I/O	Programmable I/O Alternative function : When a 32K internal crystal oscillator is used, this pin is NC	
13	GPIO2/NC	I/O	Programmable I/O Alternative function : When a 32K internal crystal oscillator is used, this pin is NC	
14	MOSI/PC00	I/O	Programmable I/O Alternative function: SPI_MOSI	
15	SCLK/PC02	I/O	Programmable I/O Alternative function: SPI_SCLK	
16	MISO/PC01	I/O	Programmable I/O Alternative function: SPI_MISO	
17	SCS/PC03	I/O	Programmable I/O Alternative function: SPI_SCS	
18	LED1	I/O	Programmable I/O Alternative function: LED1	
19	VDD	VDD	3V3	
20	GND	Vss	Power Ground	

21	LED2	I/O	Programmable I/O Alternative function: LED1
22	Res	I/O	（LED1）
23	RESET	I	RESET
24	NC		
25	GND	Vss	Power Ground
26	TDI		JTAG TDI
27	TDO_SWO		JTAG TDO_SWO
28	SWDCLK		DEBUG SWDCLK
29	SWDIO	I/O	DEBUG SWDIO
30	UART_RTS	I/O	Programmable I/O Alternative function:UART_RTS
31	UART_TX	I/O	Programmable I/O Alternative function:UART_TX
32	UART_RX	I/O	Programmable I/O Alternative function:UART_RX
33	UART_CTS	I/O	Programmable I/O Alternative function: UART_CTS
34	GND	Vss	Power Ground
35	ANT	RF	Bluetooth transmit/receive (Optional).
36	GND	Vss	Power Ground

4 PHYSICAL INTERFACE

4.1 UART Interface

FSC-BT660 UART interface is a standard 4-wire interface with RX, TX, CTS, and RTS. Supports H4 HCI interface

or raw UART to application. The default baud rate is 115.2 k baud. In order to support high and low speed baud rate, FSC-BT660 provides multiple UART clocks.

Table 4-1：Possible UART Settings

Parameter	Possible Values
Baudrate	Minimum -
	Standard 115200bps
	Maximum -
Flow control	Supports Automatic Flow Control (CTS and RTS lines)
Parity	None, Odd or Even
Number of stop bits	1
Bits per channel	8

5 MSL & ESD

Table 6-1: MSL and ESD

Parameter	Value
MSL grade:	MSL 3
ESD grade	Electrostatic discharge
ESD – Human-body model (HBM) rating, JESD22-A114-F (Total samples from one wafer lot)	Pass ±2000 V, all pins
ESD – Charge-device model (CDM) rating, JESD22-C101-D (Total samples from one wafer lot)	Pass ±500 V, all pins

6 RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccate (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the below and follow instructions specified by IPC/JEDEC J-STD-033.

Note: The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the below , the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccate and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60%RH.

Notice (注意) :

Feasycom module must use Step-Stencil, suggestion using the stencil thickness about 0.16-0.2mm,it could be modify with the product.

Table 7-1: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Feasycom surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

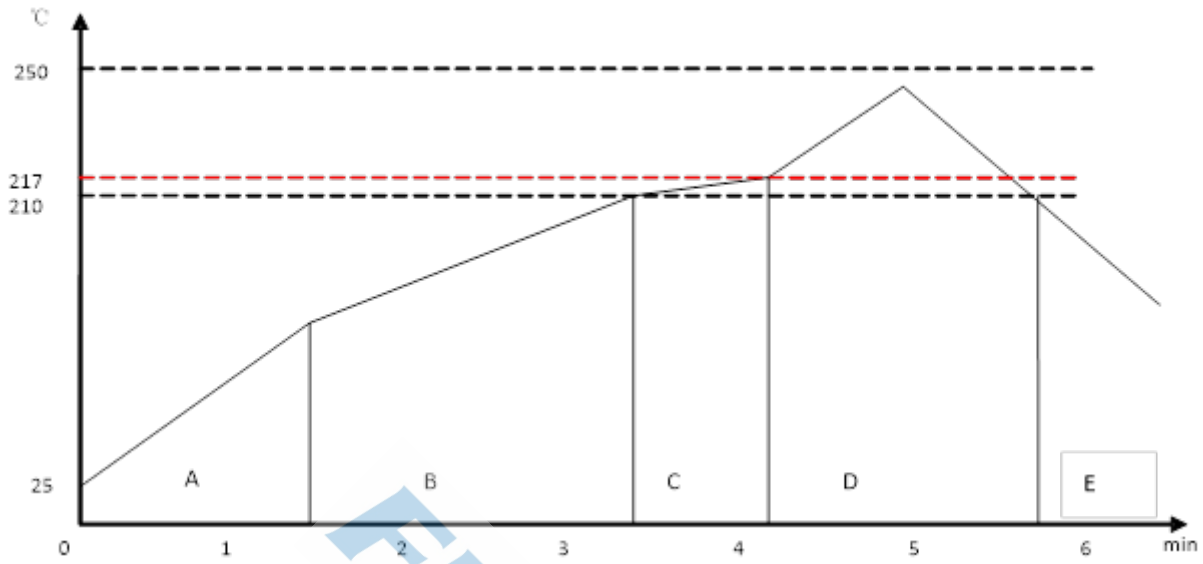

Figure 7-1：Typical Lead-free Re-flow

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

Equilibrium Zone 2 (C) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

7 MECHANICAL DETAILS

7.1 Mechanical Details

- Dimension: 12mm(W) x 15mm(L) x 1.7mm(H) Tolerance: ±0.2mm
- Module size: 12mm X 15mm Tolerance: ±0.2mm
- Pad size: 1.7mmX0.5mm Tolerance: ±0.2mm
- Pad pitch: 0.9mm Tolerance: ±0.1mm
- **(Residual plate edge error: < 0.5mm)**

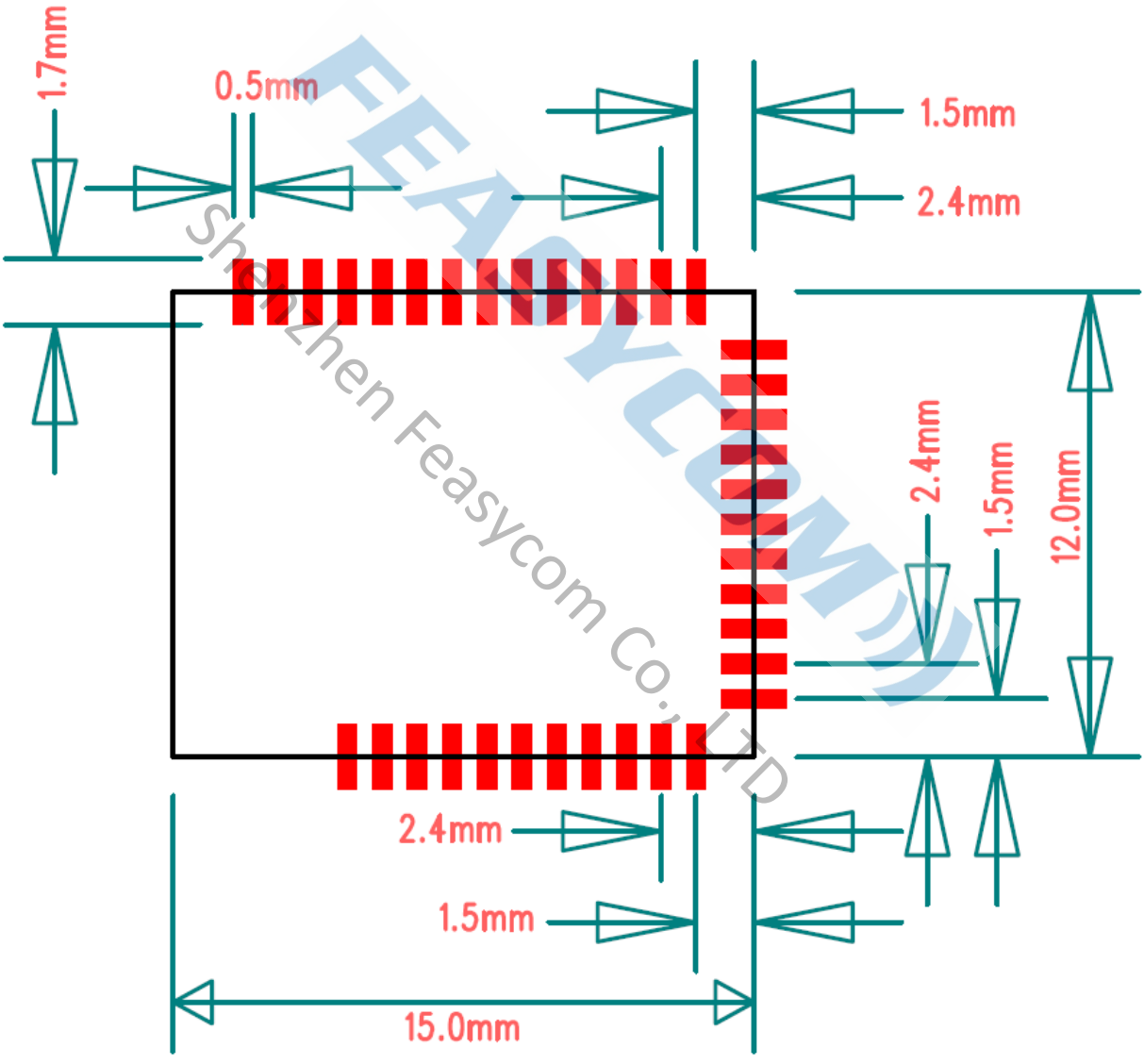

Figure 8-1: FSC-BT660 footprint Layout Guide (Top View)

8 HARDWARE INTEGRATION SUGGESTIONS

8.1 Soldering Recommendations

FSC-BT660 is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

8.2 Layout Guidelines(Internal Antenna)

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.

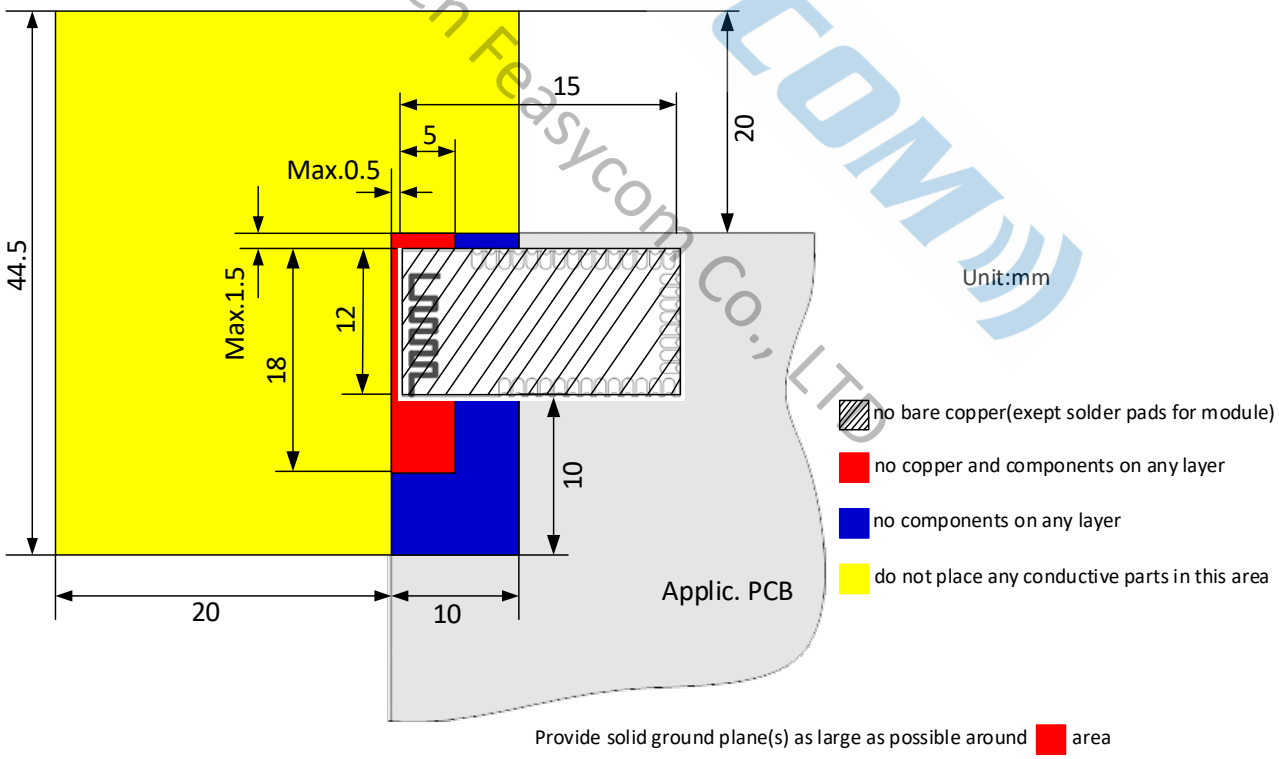

Figure 9-2: Restricted Area (Design schematic, for reference only. Unit: mm)

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid

problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

8.3 Layout Guidelines(External Antenna)

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

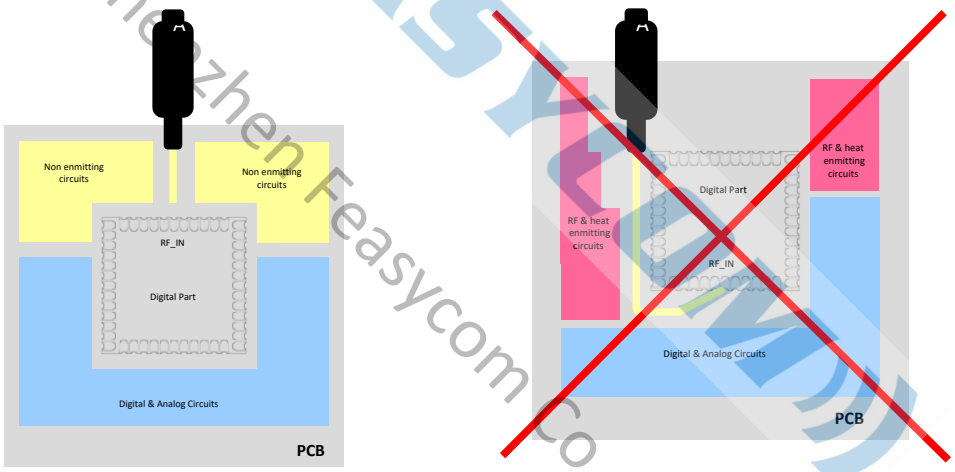

Figure 9-3: Placement the Module on a System Board

8.3.1 Antenna Connection and Grounding Plane Design

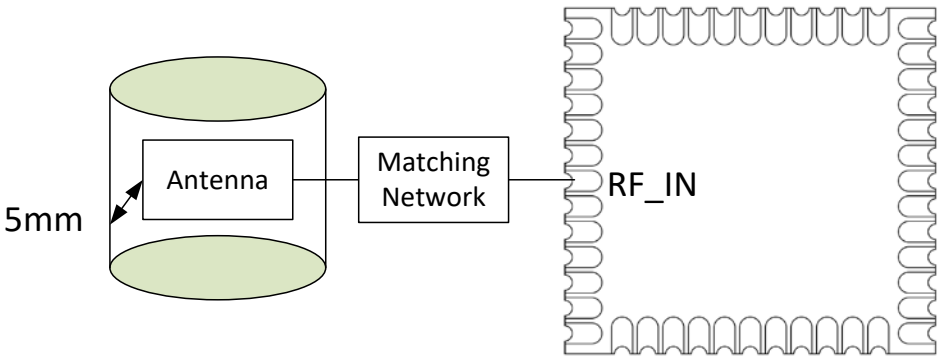

Figure 9-31-0: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

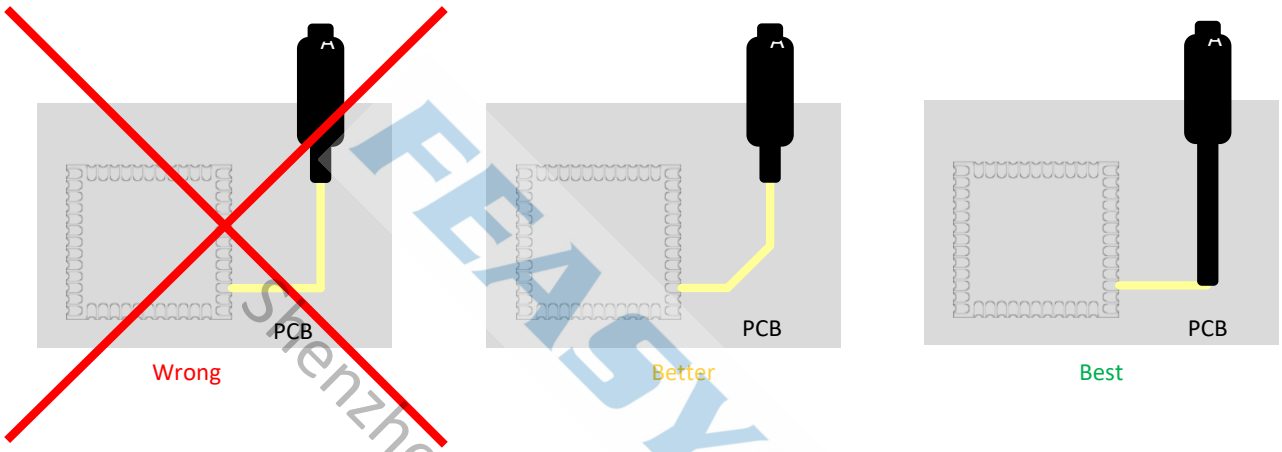

Figure 9-31-1: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

9 PRODUCT PACKAGING INFORMATION

9.1 Default Packing

Figure 10-1: Tray Dimension: 140mm * 265mm Tray vacuum

9.2 Packing box(Optional)

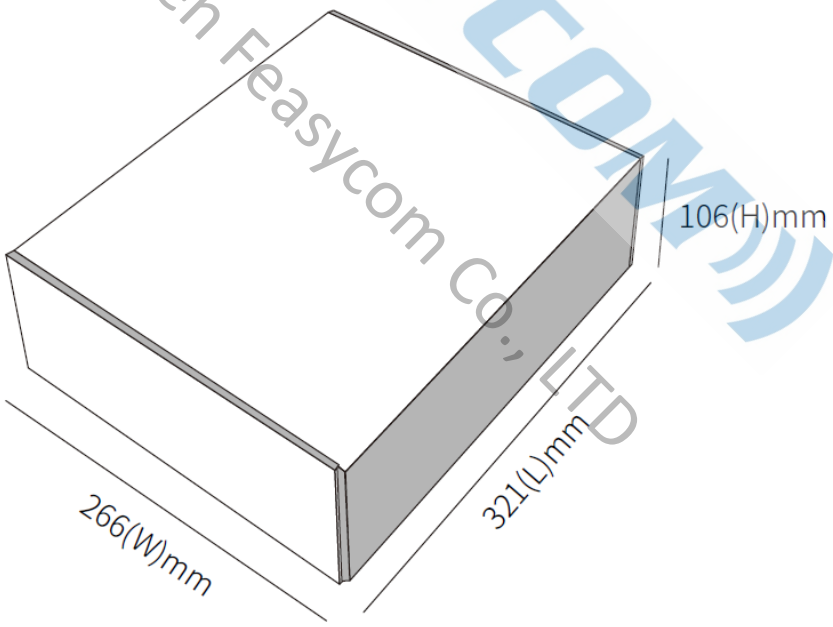

Figure 10-2: Packing box(Optional)

** If other packing is required, please confirm with the customer*

** Packing: 1000pcs per carton (Minimum packing quantity)*

** The outer packing size is for reference only, please refer to the actual size*

10 APPLICATION SCHEMATIC