FSC-BW126

IEEE 802.11ax/ac/a/b/g/n Compatible 2T2R WLAN and Integrated Bluetooth 5.2 Controller With PCI Express/HS-UART Mixed Interface Module Datasheet

Version 1.3

Revision History

Version	Data	Notes	Approved By
1.0	2022/06/24	Initial Version	Devin Wan
1.1	2022/08/23	1, Selection of version 2, Modify 5.4 PCIe Bus Power Sequence	Devin Wan
1.2	2023/03/22	Updated description of PIN36(BT_EN) and PIN37(WL_EN) in Chapter 3.2	Devin Wan
1.3	2023/08/07	Updated description of PIN45(NC/RF2_BT) (Three-antenna only Applicable to PCB version V1.1)	Devin Wan

Contact Us

Shenzhen Feasycom Co.,LTD

Email: sales@feasycom.com

Address: Rm 508, Building A, Fenghuang Zhigu, No.50, Tiezai Road, Xixiang, Baoan District, Shenzhen, 518102, China
Tel: 86-755-27924639

Contents

1. INTRODUCTION

Overview

FSC-BW126 is a highly integrated single-chip that support 2-stream 802.11ax solutions with Multi-user MIMO (Multiple-Input, Multiple-Output) with Wireless LAN (WLAN) PCI Express network interface controller and HS-UART mixed interface. It combines a WLAN MAC, a 2T2R capable WLAN baseband, and RF in a single chip. The FSC-BW126 provides a complete solution for a high-performance integrated wireless and Bluetooth device.

FSC-BW126 baseband implements Multi-user Multiple Input, Multiple Output (MU-MIMO) Orthogonal Frequency Division Multiplexing (OFDM) with two transmit and two receive paths (2T2R). Moreover, FSC-BW126 provides one spatial stream space-time block code (STBC), Transmit Beamforming (TxBF) and Low Density Parity Check (LDPC) to extend the range of transmission.

For legacy compatibility, Direct Sequence Spread Spectrum (DSSS), Complementary Code Keying (CCK) and OFDM baseband processing are included to support all IEEE 802.11b, 802.11g and 802.11a data rates. The high speed FFT/IFFT paths, combined with BPSK, QPSK, 16QAM, 64QAM, 256QAM, and up to 1024QAM modulation of the individual subcarriers, and rate compatible coding rate of 1/2, 2/3, 3/4, and 5/6, provide up to 1201Mbps for IEEE 802.11ax MIMO OFDM.

For advanced 11ax spec, FSC-BW126 can receive with OFDMA (OFDM Access) technology. The high-order modulation scheme, such as 1024-QAM, can also be handled very well. Meanwhile, diff number of total subcarrier in the HE-LTF, such as 1x, 2x and 4x is considered. More networking efficiency can be achieved by 1x, and better channel estimation performance provided by 4x.

FSC-BW126 MAC supports 802.11e for multimedia applications, 802.11i and WAPI (Wireless Authentication Privacy Infrastructure) for security, and 802.11n/ac/ax for enhanced MAC protocol efficiency. Using packet aggregation techniques such as A-MPDU with BA and A-MSDU, protocol efficiency is significantly improved. Power saving mechanisms such as Legacy Power Save, U-APSD, and MIMO power saving reduce the power wasted during idle time, and compensate for the extra power required to transmit MIMO OFDM. The FSC-BW126 provides simple legacy, 20/40/80MHz co-existence mechanisms to ensure backward and network compatibility.

Features

General

- IEEE 802.11ac compliant.
- CMOS MAC, Baseband PHY and RF in a single chip for IEEE 802.11a/b/g/n/ac/ax compatible WLAN
- Support 802.11ac 2x2,Wave-2 compliant with RX MU-MIMO
- Support 802.11ax 2x2, with OFDMA and MU-MIMO, by 4 types PPDU format, such as HE-SU-PPDU, HE-ER-SU-PPDU, HE-MU-PPDU, and HE-TB-PPDU
- Maximum PHY data rate up to 286.8 Mbps using 20MHz bandwidth, 573.5Mbps using 40MHz bandwidth, and 1201Mbps using 80MHz bandwidth
- Backward compatible with 802.11a/b/g devices while operating at 802.11n data rates
- Backward compatible with 802.11a/n/ac devices while operating at 802.11ax data rates

Host Interface

- Complies with PCI Express Base Specification Revision 1.1
- PCIe LTR/L1.Off state supported.
- Complies with HS-UART with configurable baud rate for Bluetooth

Standards Supported

- IEEE 802.11a/b/g/n/ac/ax compatible WLAN
- IEEE 802.11e QoS Enhancement (WMM)
- IEEE 802.11i (WPA, WPA2, WPA3). Open, shared key, and pair-wise key authentication services
- IEEE 802.11h DFS, TPC, Spectrum Measurement
- IEEE 802.11k Radio Resource Measurement
- WAPI (Wireless Authentication Privacy Infrastructure) certified.

MAC Features

- Frame aggregation for increased MAC efficiency (A-MSDU, A-MPDU)
- Low latency immediate Block Acknowledgement (BA)
- PHY-level spoofing to enhance legacy compatibility
- MIMO power saving mechanism
- Support TWT function for power saving.
- Channel management and co-existence
- Multiple BSSID feature allows the FSC-BW126 to assume multiple
- MAC identities when used as a wireless bridge
- Transmit Opportunity (TXOP) Short Inter-Frame Space (SIFS) bursting for higher multimedia bandwidth
- Wi-Fi Direct supports wireless peer to peer applications. Support BSR and queue size of Qos.
- Support MU EDCA feature.
- Support DFS, Channel info, PPDU state by Rx path.

Other Features

- Supports Wake-On-WLAN via Magic Packet and Wake-up frame
- Transmit Beamforming
- Support S3/S4 AES/TKIP group key update
- FTM support distance measurement
- Support Network List Offload
- CCA on secondary through RTS/CTS handshake
- Support TCP/UDP/IP checksum offload

PHY Features

- IEEE 802.11ax MIMO OFDM/OFDMA
- IEEE 802.11ac MIMO OFDM
- IEEE 802.11n MIMO OFDM
- Two Transmit and Two Receive paths
- 20MHz / 40MHz / 80MHz bandwidth transmission
- Support 2.4GHz and 5GHz band channels
- Short Guard Interval (400ns)
- Sounding packet
- DSSS with DBPSK and DQPSK, CCK modulation with long and short preamble
- OFDM with BPSK, QPSK, 16QAM, 64QAM, 256QAM and 1024QAM modulation. Convolutional Coding Rate: 1/2, 2/3, 3/4, and 5/6
- Maximum data rate 54Mbps in 802.11g, 300Mbps in 802.11n and 866.7Mbps in 802.11ac, 1201Mbps in 802.11ax.
- OFDM/DSSS receive diversity with MRC using up to 2 receive paths. Switch diversity used for CCK
- Support STBC
- Support LDPC
- Hardware antenna diversity
- Maximum-Likelihood Detection (MLD)
- Fast receiver Automatic Gain Control (AGC)
- On-chip ADC and DAC
- Build-in both 2.4GHz and 5GHz PA
- Build-in both 2.4GHz and 5GHz LNA

Bluetooth Controller

- Support Bluetooth 5 system (BT 5.2 Logo Compliant)
- Compatible with Bluetooth v2.1+EDR
- Integrated MCU to execute Bluetooth protocol stack
- Supports all packet types in basic rate and enhanced data rate
- Supports Secure Simple Pairing
- Enhanced BT/Wi-Fi Coexistence Control to improve transmission quality in different profiles
- Dual Mode support: Simultaneous LE and BR/EDR
- Supports multiple Low Energy states

Bluetooth Transceiver

- Fast AGC control to improve receiving dynamic range
- Integrated internal Class 1, Class 2, and Class 3 PA
- Supports Enhanced Power Control
- Supports Bluetooth Low Energy
- Integrated 32K oscillator for power management

Application

- Car audio and video system
- Measurement systems
- PND

Module picture as below showing

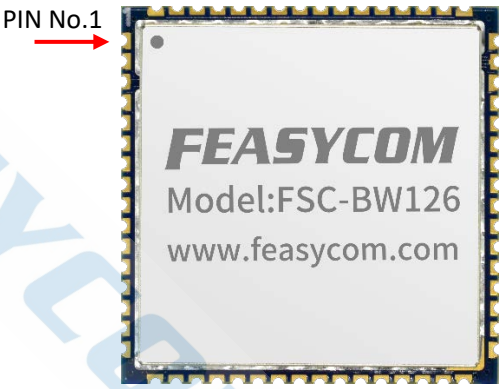


Figure 1: FSC-BW126 Picture

General Features

- Stamp module suitable for Surface Mounted Technology (SMT)
- Iron Shielding case
- Stamp-64 package
- Dimension(Iron Shielding Case) : 22mm(L) x 22mm(W) x 2.4mm(H)
- Operating Voltage :
  VBAT: 3.0 to 3.6V (Peak Current2A);
  VDDIO: 1.7 to 3.6V
- RoHS / REACH Compliant
- External Antenna
- Support Android /Linux

1.1 Selection of version

Order Number	Descriptions	Module picture as below showing
FSC-BW126	Operating temperature：-10°C ~+70°C	
FSC-BW126B	Operating temperature：-40°C ~+85°C	

2. General Specification

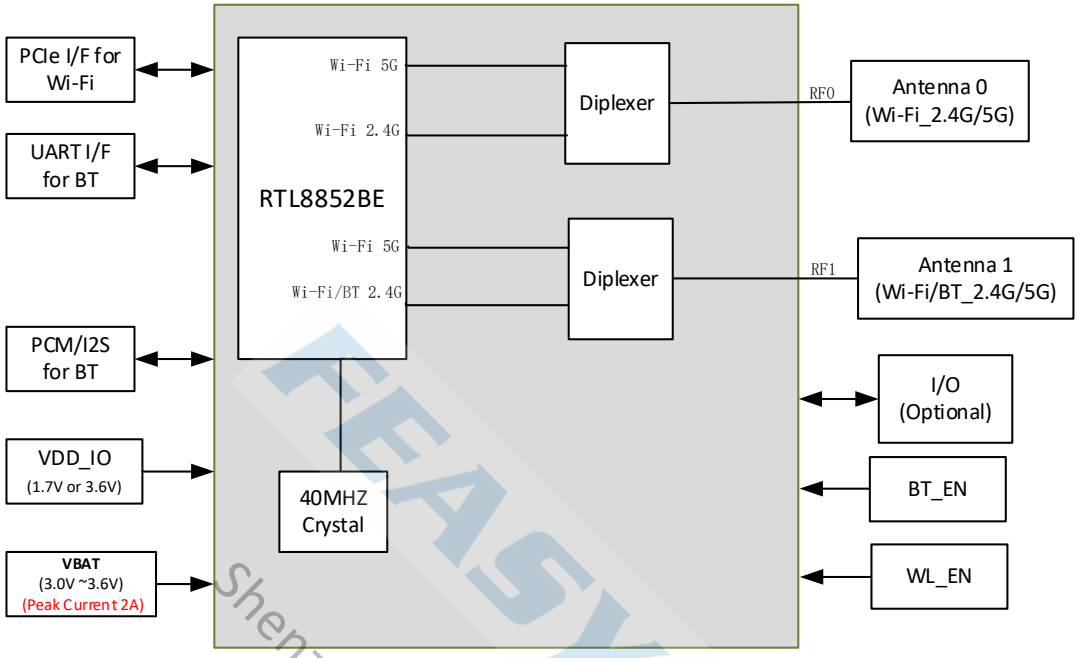
Table 1: General Specifications

Categories	Features	Implementation
Bluetooth		
Bluetooth Specification		Bluetooth V5.2 Dual-mode
Frequency Band		2402MHz~2480MHz
Bluetooth class		Class 1, Class 2,Class 3
Range, line of sight		>10m
Transmit power		12dBm (Max.)
Receiver sensitivity		-90dBm (GFSK, 0.1% BER, 1 Mbps) -92dBm (π/4-DQPSK, 0.01% BER, 2 Mbps) -86dBm (8-DPSK, 0.01% BER, 3 Mbps)
Support mode		Slave and Master
Profiles		Support HFP, A2DP, AVRCP, PBAP, SPP, MAP, DUN, PAN, FTP, GATT and etc. (when Feasycom Bluetooth stack running in host platform)
Maximum throughput		2, 3Mbps
LE Spacing		1MHz / 2MHz
Interface		UART/PCM

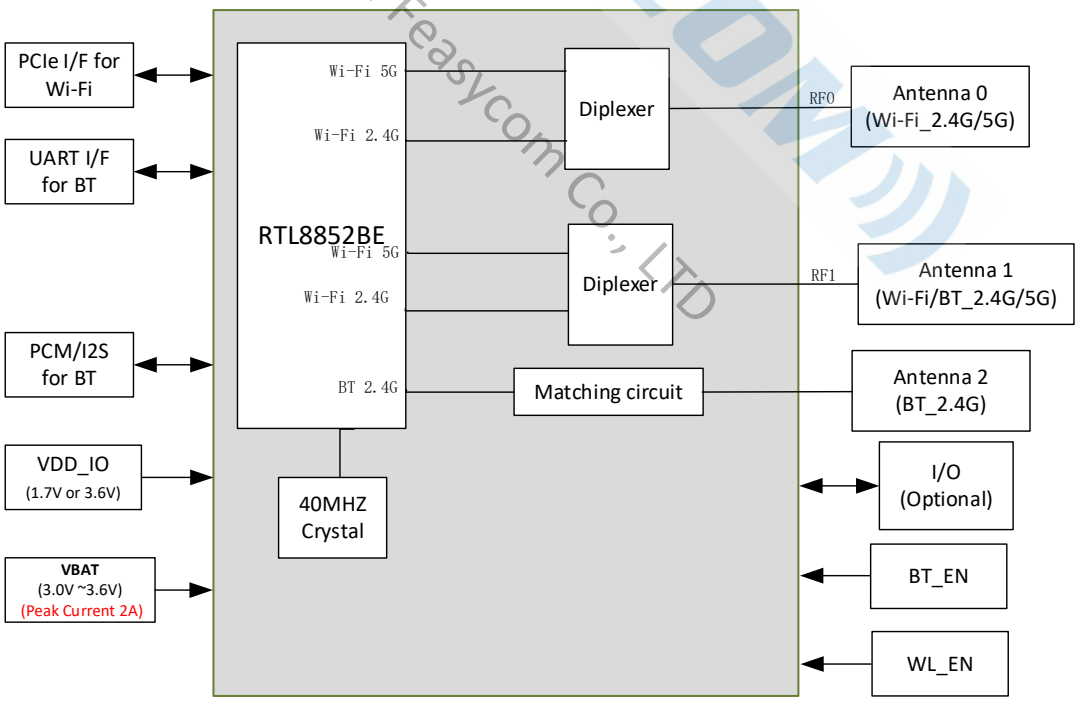
Wi-Fi		
Wi-Fi feature		2.4G: IEEE802.11 b/g/n/ac/ax 5G: IEEE802.11 a/n/ac/ax
Range, line of sight		Up to 100m
Frequency Band		2.4GHz and 5GHz frequency band
Transmit power		19dBm@802.11b (Max.) 18dBm@802.11a (Max.) 13dBm@802.11ax 2.4G & 5G (Min.)
Receiver sensitivity		-91dBm@802.11bg_1ss_BW-20 CCK 11M -78dBm@802.11bg_1ss_BW-20 OFDM 54M -72dBm@802.11n_1ss_BW-40/20 MCS7 -66.5dBm@802.11ac_1ss_ BW-40/20 MCS9 -63.7dBm@802.11ax_1ss_ BW-40/20 MS11 -72.5dBm@802.11an_1ss_Sensitivity_BW-80/40/20 MCS9 -63.5dBm@802.11ac_1ss_Sensitivity_BW-80/40/20 MCS9 -60.5dBm@802.11ax_1ss_Sensitivity_BW80/40/20 MS11
Profiles		Wi-Fi-AP(access point), Wi-Fi-Station, Wi-Fi-P2P
Maximum throughput		802.11b:Up to 11Mbps 802.11g:Up to 54Mbps 802.11n:Up to 286.8Mbps 802.11ac:Up to 573.5 Mbps 802.11ax:Up to 1201Mbps
Security		Support S3/S4,TKIP, AES, WPA, WPA2,WAP3,WMM
Interface		PCIe
General		
Size		22mm(L) x 22mm(W) x 2.4mm(H)
Hardware Interface		UART, GPIO, PCIe, PCM
Antenna		External (2.4GHz&5.8GHz dual-mode antenna)
Operating temperature		-10°C ~+70°C or -40°C ~+85°C *Note: See chapter 1.1 for details*
Storage temperature		-40°C ~+85°C
Operating voltage (VBAT)		3.3V (Typ.) (Peak Current2A)
VDDIO		1.8V/3.3V(Typ.)
Miscellaneous	Lead Free	Lead-free and RoHS compliant
	Warranty	One Year
Humidity		10% ~ 90% non-condensing
MSL grade:		MSL 3
ESD grade:		Human Body Model: Pass ±2000 V, all pins Charge device model: Pass ±250 V, all pins

3. HARDWARE SPECIFICATION

3.1 Block Diagram and PIN Diagram



Two-antenna



Three-antenna

Figure 2: Block Diagram

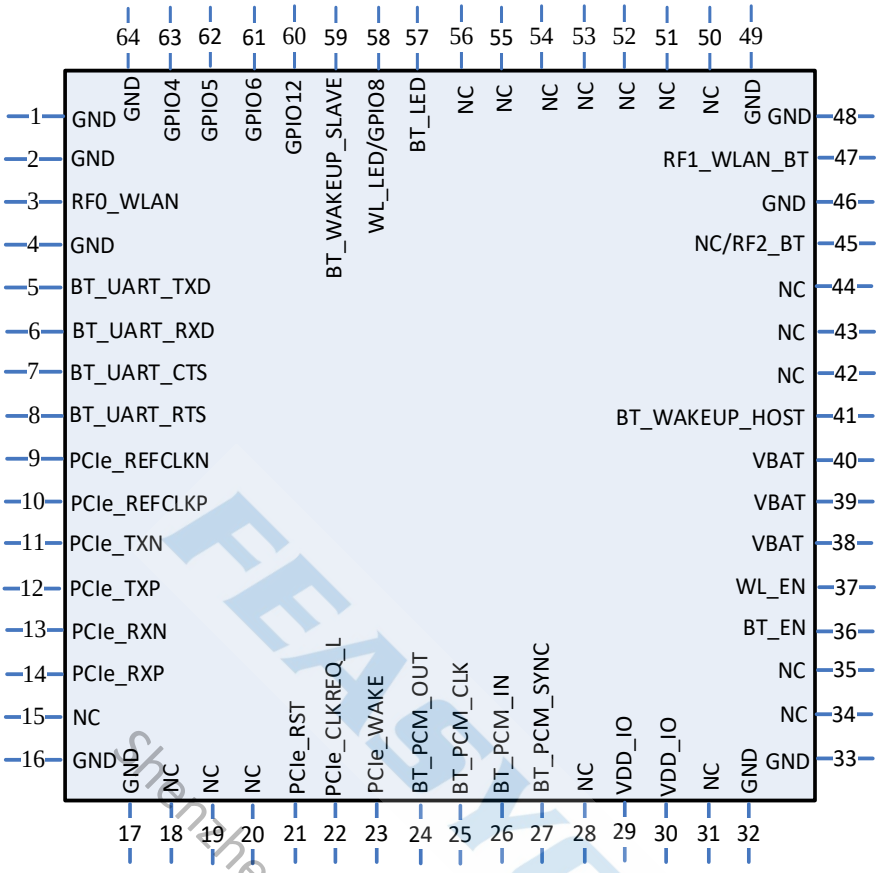


Figure 3: FSC-BW126 PIN Diagram (Top View)

3.2 PIN Definition Descriptions

Table 2: Pin definition

Pin	Pin Name	Type	Pin Descriptions	Notes
1	GND	VSS	Ground	
2	GND	VSS	Ground	
3	RF0_ WLAN	RF	WLAN 2.4/5GHz and RF input/output port for chain 0	
4	GND	VSS	Ground	
5	BT_UART_TXD	O	BT UART serial output	
6	BT_UART_RXD	I	BT UART serial input	
7	BT_UART_CTS	O	BT UART clear-to-send	
8	BT_UART_RTS	I	BT UART request-to-send	
9	PCIe_REFCLKN	I	PCIe differential clock inputs (negative), 100MHz ± 300ppm differential	
10	PCIe_REFCLKP	I	PCIe differential clock inputs (positive), 100MHz ± 300ppm differential.	
11	PCIe_TXN	O	PCI Express Transmit Differential Pair	
12	PCIe_TXP	O	PCI Express Transmit Differential Pair	
13	PCIe_RXN	I	PCI Express Receive Differential Pair	
14	PCIe_RXP	I	PCI Express Receive Differential Pair	
15	NC			
16	GND	VSS	Ground	

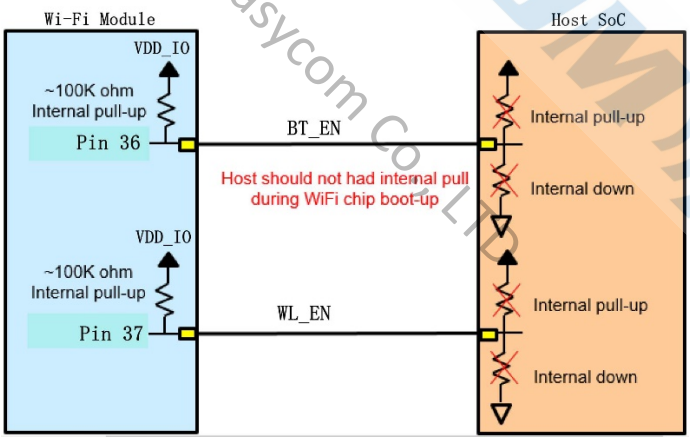
17	GND	VSS	Ground	
18	NC			
19	NC			
20	NC			
21	PCIe_RST	I	PCI Express Reset Signal: active low. When the PERST# is asserted at power-on state, the module returns to a pre-defined reset state and is ready for initialization and configuration after the de-assertion of the PERST#. **(The pin must be 3.3V; VDD_IO input to 1.7V or 3.6V)**	
22	PCIe_CLKREQ_L	I/O/D	Reference clock request **(The pin must be 3.3V; VDD_IO input to 1.7V or 3.6V)**	
23	PCIE_WAKE	O/D	Power Management Event: Open drain, active low. Used to reactivate the PCI Express slot's main power rails and reference clocks. This WAKE# can be shared with BT wake up host function via sideband signals. **(The pin must be 3.3V; VDD_IO input to 1.7V or 3.6V)**	
24	BT_PCM_OUT	O	BT PCM output signal	
25	BT_PCM_CLK	I/O	BT PCM clock signal	
26	BT_PCM_IN	I	BT PCM input signal	
27	BT_PCM_SYNC	I/O	BT PCM synchronization signal	
28	NC			
29	VDD_IO	I/O	1.7Vor 3.6V(Input); Connect to 1.7V or 3.6V external power	
30	VDD_IO	I/O	1.7Vor 3.6V(Input); Connect to 1.7V or 3.6V external power	
31	NC			
32	GND	VSS	Ground	
33	GND	VSS	Ground	
34	NC			
35	NC			
36	BT_EN	I	Bluetooth Function Enable (VDD_IO input to 1.7V or 3.6V) **There is internal pull-up, about 100K.**	**Note 1**
37	WL_EN	I	Wi-Fi Function Enable (VDD_IO input to 1.7V or 3.6V) **There is internal pull-up, about 100K.**	**Note 1**
38	VBAT	PWR	Module Main Power Input (3.3V)	
39	VBAT	PWR	Module Main Power Input (3.3V)	
40	VBAT	PWR	Module Main Power Input (3.3V)	
41	BT_WAKEUP_HOST	O	Bluetooth wakeup the host, active high. NC if not used.	
42	NC			
43	NC			
44	NC			
45	NC/RF2_BT	RF	NC /Bluetooth RF input/output port chain 2 *(Three-antenna only)*	
46	GND	VSS	Ground	
47	RF1_ WLAN_BT	RF	WLAN 2.4 / 5GHz and Bluetooth RF input/output port chain 1	
48	GND	VSS	Ground	

49	GND	VSS	Ground
50	NC		
51	NC		
52	NC		
53	NC		
54	NC		
55	NC		
56	NC		
57	BT_LED	O	BT LED Pin (Active Low). NC if not used.
58	WL_LED/GPIO8	O	WL LED Pin (Active Low), shared with GPIO8. NC if not used.
59	BT_WAKEUP_SLAVE	I	Host wakeup Bluetooth, active high. NC if not used.
60	GPIO12	I/O	NC if not used. (The Host wakes up the WLAN controller in Remote Wakeup Mode. We suggest configuring the control pin in in platform side as open-drain.)
61	GPIO6	I/O	NC if not used.
62	GPIO5	I/O	NC if not used.
63	GPIO4	I/O	NC if not used.
64	GND	VSS	Ground

Note 1

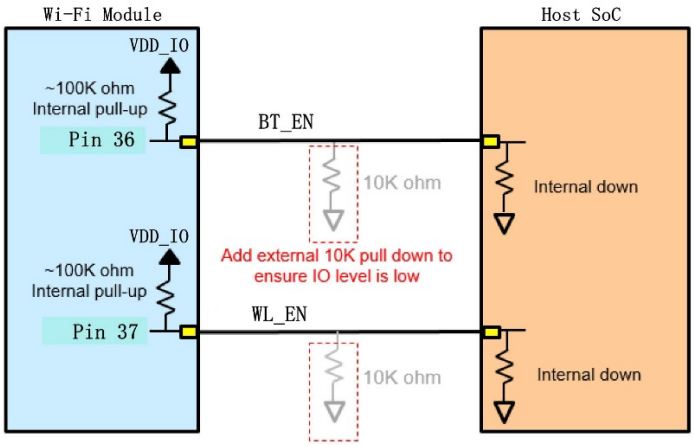
There is internal pull-up, about 100K, resistor design in Pin36(BT_EN) and Pin37(WL_EN) pad.

If Host SOC need to control these two pins, choose host GPIO without pull capability to avoid voltage divider. Middle range of IO voltage would affect Wi-Fi booting up.



Add external pull down resistor to ensure low level

If Host GPIO has pull-down capability and it can't be avoided, suggest to add 10K pull down resistor in circuit to ensure IO is in low level. In this way, Wi-Fi chip internal pull-up 100K could be neglected. Please note external pull-down will cause additional static current.



Add external pull down resistor to ensure low level

4. UART Interface Characteristics

The UART interface is a 3-wire interface with RX, TX, CTS. The interface supports the Bluetooth 2.0 UART HCI H4 and H5 specifications. The default baud rate is 115.2k baud. In order to support high and low speed baud rate, the FSC-BW126 provides multiple UART clocks.

The UART signal level ranges from 1.8V or 3.3V.

The interface includes four signals, TXD/RXD/CTS. Flow control between the host and the device is byte-wise by hardware. When the UART_CTS signal is set high, the device stops transmitting on the interface. If HCI_CTS is set high in the middle of transmitting a byte, the device finishes transmitting the byte and stops the transmission.

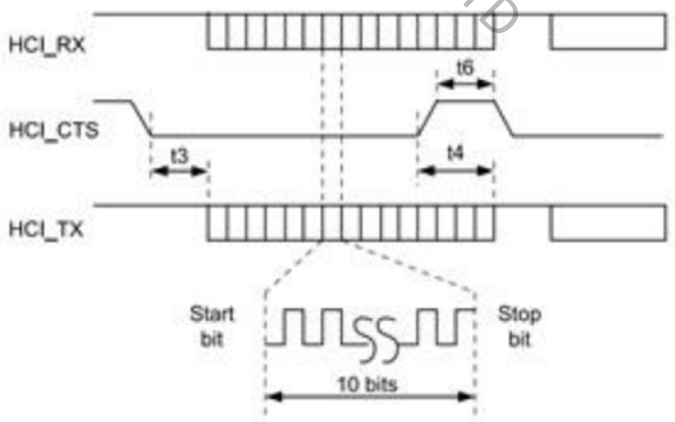


Figure 4: UART Timing Diagram

Table 3: UART Timing Specifications

Parameter	Symbol	Min	Type	Max	Unit
Baud rate		115.2		3000	Kbps
Baud rate accuracy per (Receive/Transmit)		-3		3	%
CTS low to TX_DATA on	T3	0	2		ns
CTS high to TX_DATA off (Hardware flow)	T4			1	byte
CTS High Pulse Width	T6	1			byte

Note : HCI packet means HCI command(256 bytes), HCI event(256 bytes), ACL(1024 bytes), SCO(256 bytes)

The UART interface power-on sequence differs depending on whether or not host flow control is supported.

UART Hardware Flow Control Not Supported

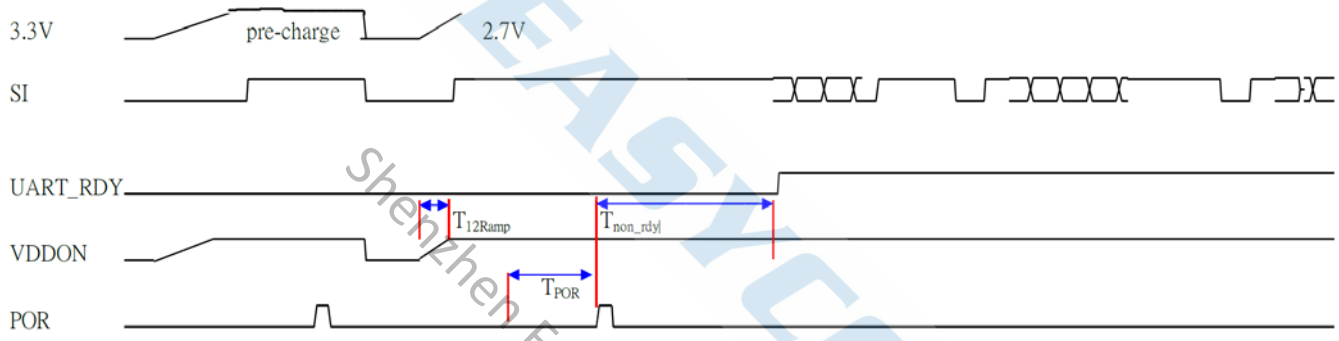


Figure 5: UART Power-On Sequence Without Hardware Flow Control

UART Hardware Flow Control Supported

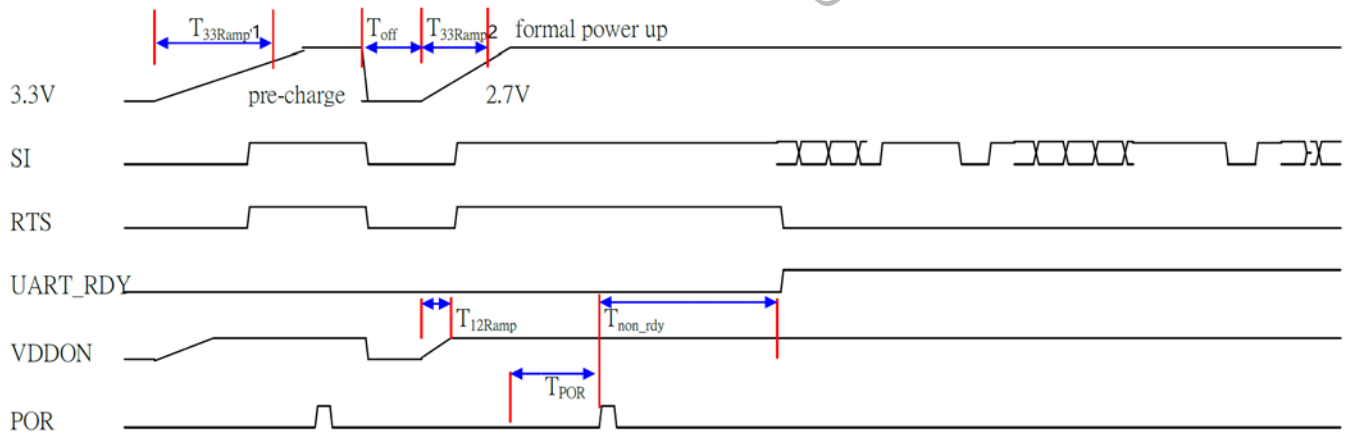


Figure 6: UART Power On Sequence With Hardware Flow Control

Table 4: UART Interface Power-On Sequence

Symbol	Description
$T_{33ramp}1$	3.3V Power Pre-Charge Ramp Up Duration Before Formal Power Up. We recommend that a 3.3V power-on and then power-off sequence is executed by the host controller before the formal power on sequence. This procedure can eliminate host card detection issues when power ramp up duration is too long, or when a system warm reboot fails.
T_{off}	The duration 3.3V is cut off before formal power up.
$T_{33ramp}2$	The 3.3V main power ramp up duration.
T_{12ramp}	The internal 1.2V ramp up duration.
T_{POR}	The duration from when the power-on reset releases and the power management unit executes power on tasks. A power on reset will detect both 3.3V and 1.2V power ramp up after a predetermined duration.
T_{non_rdy}	UART Not Ready Duration. In this state, the module will not respond to any commands.

We recommend that the card detection procedures are divided into two phases: A 3.3V power pre-charge phase and a formal power-up phase.

During the 3.3V power pre-charge phase, the power ramp up duration is not limited. The 3.3V power is cut off and is turned on after the T_{off} period. The ramp up time is specified in the T_{33ramp} duration.

After main 3.3V ramp up and 1.2V ramp up, the power management unit is enabled by the power ready detection circuit. The power management unit enables the Bluetooth block. The Bluetooth firmware then initializes all circuits included the UART.

Table 5: UART Interface Power On Timing Parameters

Parameter	Min	Type	Max	Unit
$T_{33ramp}1$	-	-	No Limit	ms
T_{off}	250	500	1000	ms
$T_{33ramp}2$	0.1	0.5	2.5	ms
T_{12ramp}	0.1	0.5	1.5	ms
T_{POR}	2	2	8	ms
T_{non_rdy}	1	2	10	ms

5. ELECTRICAL CHARACTERISTICS

5.1 Recommended Operating Conditions

Table 6: Recommended Operating Conditions

Parameter	Min	Type	Max	Unit
VBAT （Peak Current：2A）	3.0	3.3	3.6	V
VDDIO	1.7	1.8/3.3	3.6	V
Operating temperature (T_A) ***Note**	-10	25	+70	℃
Storage temperature (T_{stg})	-40	25	+85	℃

- **Note: See chapter 1.1 for details*

5.2 Platform State Transitions

Table 7: PCIE Platform Power Rail Requirements

3.3V Power range	3.3V Ripple	3.3V Noise	Rise time Min	Rise time Max
+/-0.165V	300mVpp @ switching frequency > 100KHz		0.5ms	5ms

5.3 Digital IO Pin DC Characteristics

Table 8: 3.3V IO DC Characteristics

Parameter	Min	Type	Max	Unit
V_{IH} -Input high voltage	2.0	3.3	3.6	V
V_{IL} -Input low voltage	-	0	0.9	V
V_{oH} -Output high voltage	2.97	-	3.3	V
V_{oL} -Output low voltage	0	-	0.33	V

Table 9: 1.8V IO DC Characteristics

Parameter	Min	Type	Max	Unit
V_{IH} -Input high voltage	1.7	1.8	3.6	V
V_{IL} -Input low voltage	-	0	0.8	V
V_{oH} -Output high voltage	1.62	-	1.8	V
V_{oL} -Output low voltage	0	-	0.18	V

5.4 PCIe Bus Power Sequence

a. When WLAN is power off

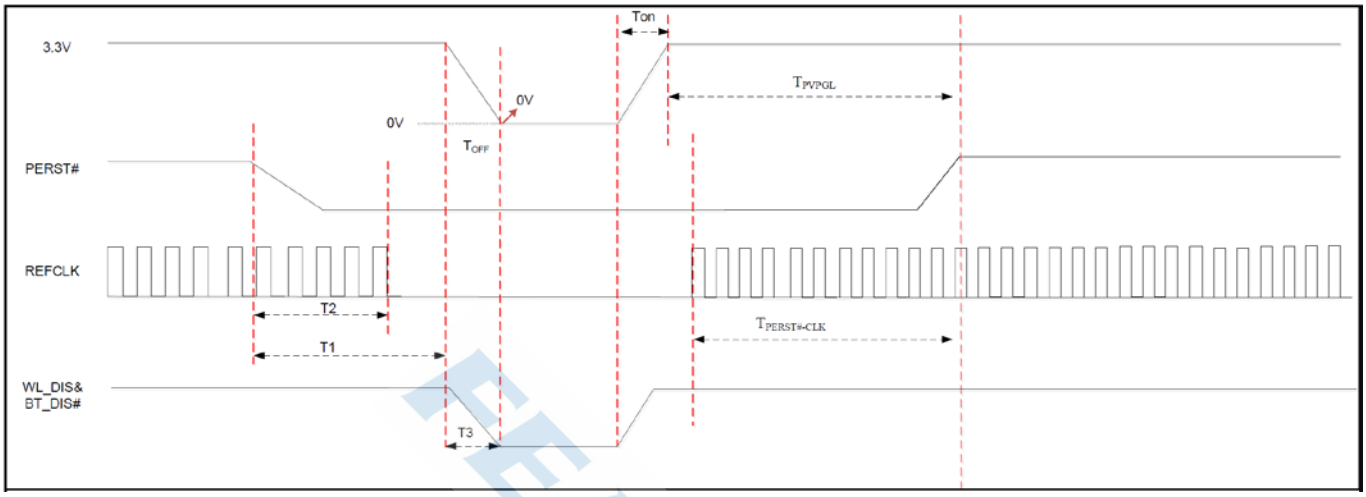


Figure 7: When WLAN is power off

b. When WLAN is NOT power off

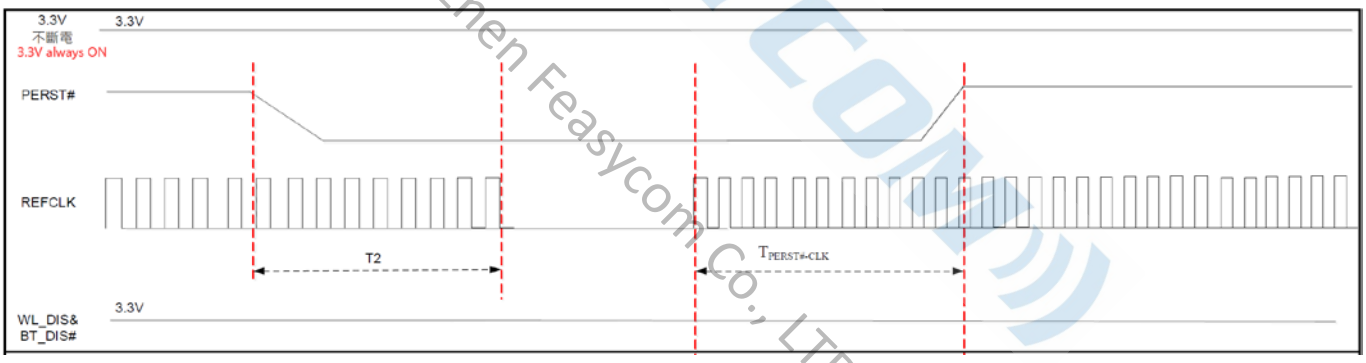


Figure 8: When WLAN is NOT power off

T_{on}: The main power ramp up duration

T_{off}: The main power off duration

T_{PVPGL}: Power valid to PERST# input inactive

$T_{PERST\#-CLK}$: Reference clock stable before PERST# inactive

Note:

1. PERST#=PCIe_RST; REFCLK=PCIe_REFCLK; WL_DIS&BT_DIS#=WL_EN&BT_EN;
2. T1: PERST# goes active before the power on the connector is removed.
3. T2: Clock to inactive after PERST# goes active.
4. T3: WL_DIS# and BT_DIS# goes asserted when the power on the connector is removed.
5. T1/T2/T3 timing value should large than 0.

Table 10: PCIE typical timing range

Symbol	Min	Type	Max	Unit
T_{on}	0.5	1.5	5	ms
T_{off}	1.5	-	-	ms
T_{PVPGL}	Implementation specific; recommended 50ms	-	-	ms
$T_{PERST\#-CLK}$	100	-	-	us

5.5 PCIe PERST# Timing Sequence (if need at least twice)

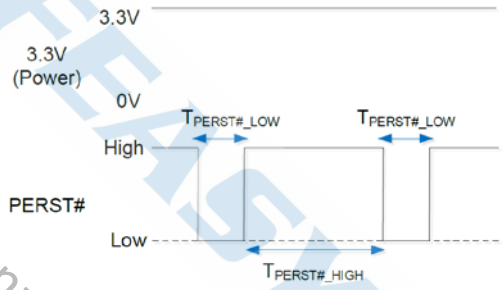


Figure 9: PCIe PERST# Timing Sequence (if need at least twice)

Table 11: PCIE PERST# Timing Parameters

Symbol	Min	Type	Max	Unit
$T_{PERST\#-LOW}$ (PERST# low duration)	6	10	~	ms
$T_{PERST\#-HIGH}$ (PERST# high duration)	400	500	~	ms
Note: PERST#=PCIe_RST;				

5.6 Power Off Sequence

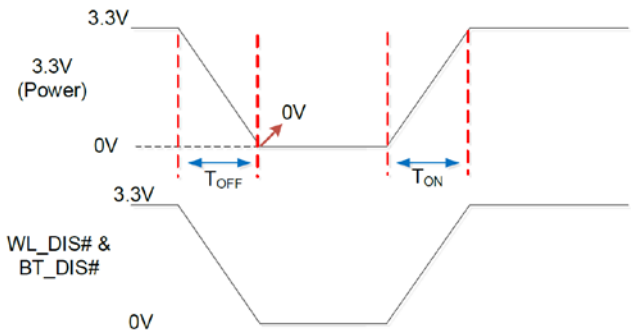


Figure 10: Power OFF Sequence of 3.3V platform

Note:

1. WL_DIS&BT_DIS#=WL_EN&BT_EN;
2. If BT_DIS# can't connect to the same power source with 3.3V, it need to be de-asserted before PERST# with 100ms in power on sequence.

Table 12: Power Off Timing Parameters of 3.3V platform

Symbol	Min	Type	Max	Unit
T_{OFF} Measure point start on 100% Measure point end on 0% (must be 0V)	1.5	-	-	ms
T_{ON} Measure point start on 0% (must be 0V) Measure point end on 100%	0.5	1.5	5	ms

5.7 BT_EN Timing Sequence

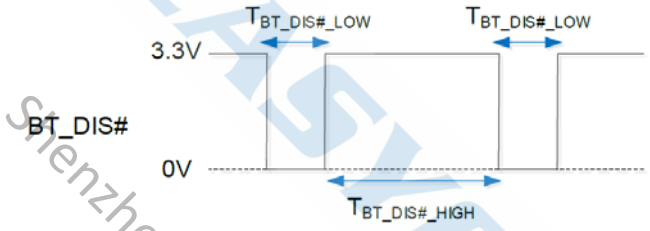


Figure 11: BT_EN Timing Sequence

Note:

1. BT_DIS#= BT_EN;

Table 13: Power Off Timing Parameters of 3.3V platform

Symbol	Min	Type	Max	Unit
BT_DIS#_LOW (BT_DIS# low duration)	200	-	-	ms
BT_DIS#_HIGH (BT_DIS# high duration)	500	-	-	ms

5.8 Module Hardware Configuration and Application Circuit for 1.8V I/O Platform

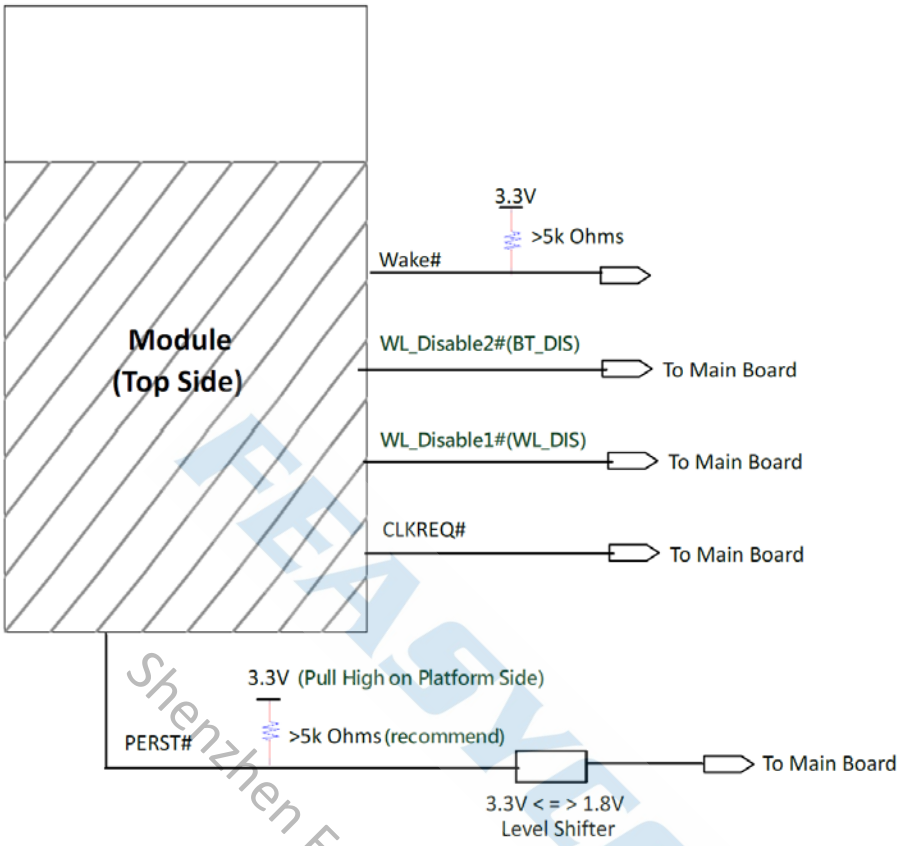


Figure 12: Power OFF Sequence of 3.3V platform

Note:
1. Wake#=PCIe_WAKE; CLKREQ#=PCIe_CLKREQ_L; WL_DIS=WL_EN; BT_DIS=BT_EN; PERST#=PCIe_RST;
2. Module side WAKE# doesn't need to pull high. System side/Platform need to pull high (1.8V or 3.3V).
3. Module side WL/BT_Disable# internal pull high to 3V3 and connect to golden pin. System side /Platform can floating and don't connect to module side.

5.9 PCIE differential traces and layout guide

A , AC coupled Cap. Circuit & Layout Consideration

- AC Couple Cap. Requirement for HSOP/HSON differential pairs:

  Gen1/Gen2: 75nF~175nF, 100nF typ.
  Gen3: 176nF~265nF, 220nF typ.
- Place AC coupling capacitors near output pins of HSOP/HSON differential pairs.

B , Layout trace impedance control

- TX/RX: Gen1: 100 Ohms +/- 10%
- CLK: 100 Ohms +/- 10%

C , Differential trace Intra-Pair skew Layout requirement

- Mismatch Requirement:

Host (Both TX/RX pairs) : < 10mil
Device (Both TX/RX pairs): < 5mil

- Serpentine lines routing can be permitted, but should be routed as the following rules.

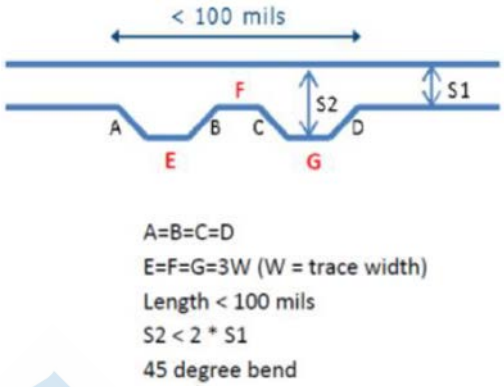


Figure 13: Serpentine lines Routing Rules

5.10 RF Characteristic

5.10.1 WLAN RF Characteristics(Transmitter)

Table 14: WLAN Transmitter

Characteristics	Condition		Min	Type	Max	Unit
2.4GHz		EVM	2400		2500	MHz
Output Power	802.11b_1ss_CCK_11M	-4.6dB		19.5	19.5	dBm
	802.11g_1ss_OFDM_54M	-34dB		18	19.5	dBm
TX power at the chip port for highest power level setting at 25°C and VBAT = 3.3V with spectral mask and EVM compliance	802.11n_1ss_HT20_MCS7	-35dB		17	19	dBm
	802.11n_1ss_HT40_MCS7	-36dB		17	19	dBm
	802.11ac_1ss_VHT20_MCS8	-36dB		16	19	dBm
	802.11ac_1ss_VHT40_MCS9	-38 dB		15	19	dBm
	802.11ax_1ss_SU-HE20_MCS11	-38 dB		13	19	dBm
	802.11ax_1ss_SU-HE40_MCS11	-38dB		13	19	dBm
5GHz			4900		5845	MHz
Output Power	802.11a_1ss_OFDM_54M	-35 dB		18	19	dBm
	802.11n_1ss_VHT20_MCS7	-37 dB		17	19	dBm
TX power at the chip port for highest power level setting at 25°C and VBAT = 3.3V with spectral mask and EVM compliance	802.11n_1ss_VHT40_MCS7	-36 dB		17	19	dBm
	802.11ac_1ss_VHT20_MCS8	-38dB		16	19	dBm
	802.11ac_1ss_VHT40_MCS9	-38dB		15	19	dBm
	802.11ac_1ss_VHT80_MCS9	-35dB		15	19	dBm
	802.11ax_1ss_SU-HE20_MCS11	-40dB		13	19	dBm
	802.11ax_1ss_SU-HE40_MCS11	-39dB		13	19	dBm
	802.11ax_1ss_SU-HE80_MCS11	-38dB		13	19	dBm

5.10.2 WLAN RF Characteristics(Receiver)

Table 15: WLAN Receive

Characteristics	Condition	Min	Type	Max	Unit
2.4GHz		**2400**		**2500**	**MHz**
Sensitivity	802.11bg_1ss_BW-20 CCK 11M	-91		-91.5	dBm
	802.11bg_1ss_BW-20 OFDM 54M	-78		-79	dBm
	802.11n_1ss_BW-40/20 MCS7	-72.0		-76.5	dBm
	802.11ac_1ss_ BW-40/20 MCS9	-66.5		-72	dBm
	802.11ax_1ss_ BW-40/20 MS11	-63.7		-67.5	dBm
5GHz		**4900**		**5845**	**MHz**
Sensitivity	802.11an_1ss_Sensitivity_BW-80/40/20 MCS9	–72.5		–78.5	dBm
	802.11ac_1ss_Sensitivity_BW-80/40/20 MCS9	–63.5		-72.5	dBm
	802.11ax_1ss_Sensitivity_BW80/40/20 MS11	–60.5		–67.5	dBm

5.10.3 Bluetooth RF Characteristics

Table 16: Bluetooth RF Characteristics

Characteristics	Condition	Min	Type	Max	Unit
Bluetooth specification	Version 5.2				
Channel frequency (spacing)	2402 to 2480 MHz (1MHz)				
BT Transmitter, GFSK					
RF output power	Basic rate (GFSK) TX power		10	12	dBm
	QPSK TX Power		9	10	dBm
	8PSK TX Power		9	10	dBm
Power control step		2	4	8	dB
BT Receiver Characteristics, Basic rate receiver					
RX sensitivity	GFSK, BER = 0.1%, 1 Mbps		-90	-91	dBm
	π/4-DQPSK, BER = 0.01%, 2 Mbps		-92	-93	dBm
	8-DPSK, BER = 0.01%, 3 Mbps		-86	-87	dBm
Input IP3		-16			dBm
Maximum input at RF port				-20	dBm
BLE RF Characteristics					
BLE Transmitter output power			9	10	dBm
BT Receiver Characteristics, Low energy receiver	GFSK, 0.1% BER, 1Mbps		-94	-96	dBm

Notes:

1. Dirty TX is OFF
2. The Bluetooth LE TX power cannot exceed 10dBm EIRP specification limit. The front-end losses and antenna gain/loss

must be factored in so as not to exceed the limit.

6. MSL & ESD

Table 17: MSL and ESD

Parameter	Value
MSL grade:	MSL 3
ESD grade	**Electrostatic discharge**
ESD – Human Body Model (HBM) Rating JESD22-A114-B	Pass ±2000 V, all pins
ESD – Charged Device Model (CDM) Rating JESD22-C101-D	Pass ±250 V, all pins

7. RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccate (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the below and follow instructions specified by IPC/JEDEC J-STD-033.

Note: The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the below , the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccate and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60%RH.

Notice (注意) :

Feasycom module must use Step-Stencil, suggestion using the stencil thickness about 0.16-0.2mm,

it could be modify with the product.

使用我司模块，须使用阶梯钢网，建议阶梯钢网厚度0.16-0.20mm，可根据自己产品适应性，进行相应调整.

Table 18: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Feasycom surface mount modules conform to

J-STD-020D1 standards for reflow temperatures.

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

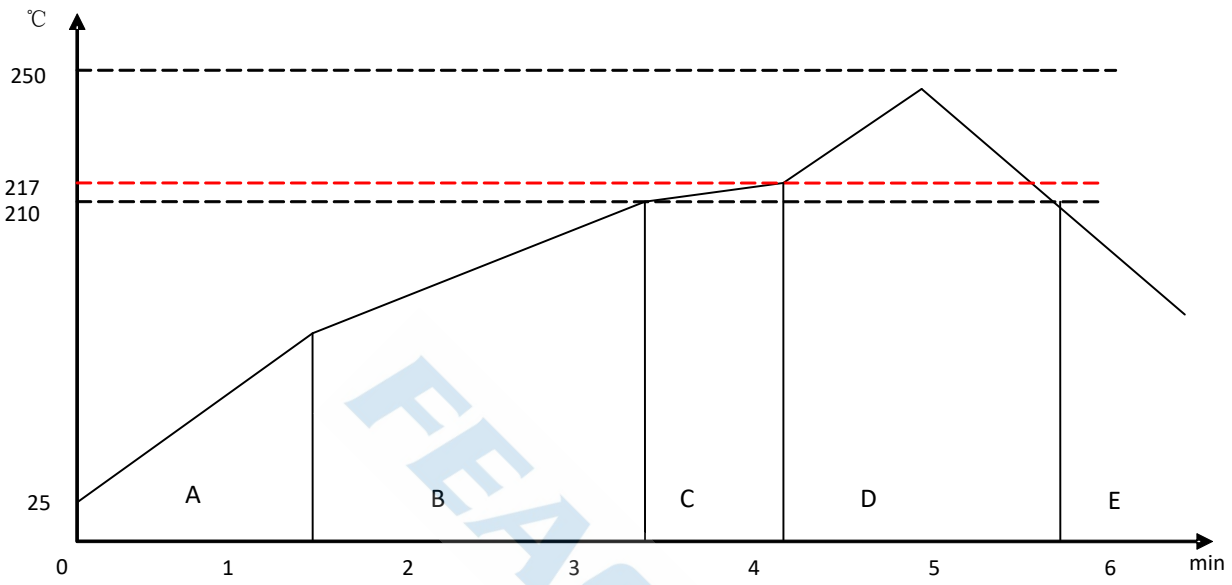


Figure 14: Typical Lead-free Re-flow

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

Equilibrium Zone 2 (C) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

8. MECHANICAL DETAILS

8.1 Mechanical Details

- Dimension: 22mm(L) x 22mm(W) x 2.4mm(H) Tolerance: ±0.2mm
- Module size: 22mm x 22mm Tolerance: ±0.25mm
- Pad size: 1.8mmX0.8mm Tolerance: ±0.1mm
- Pad pitch: 1.2mm ±0.1mm

(分板后边角残留板边误差：不大于0.5mm)

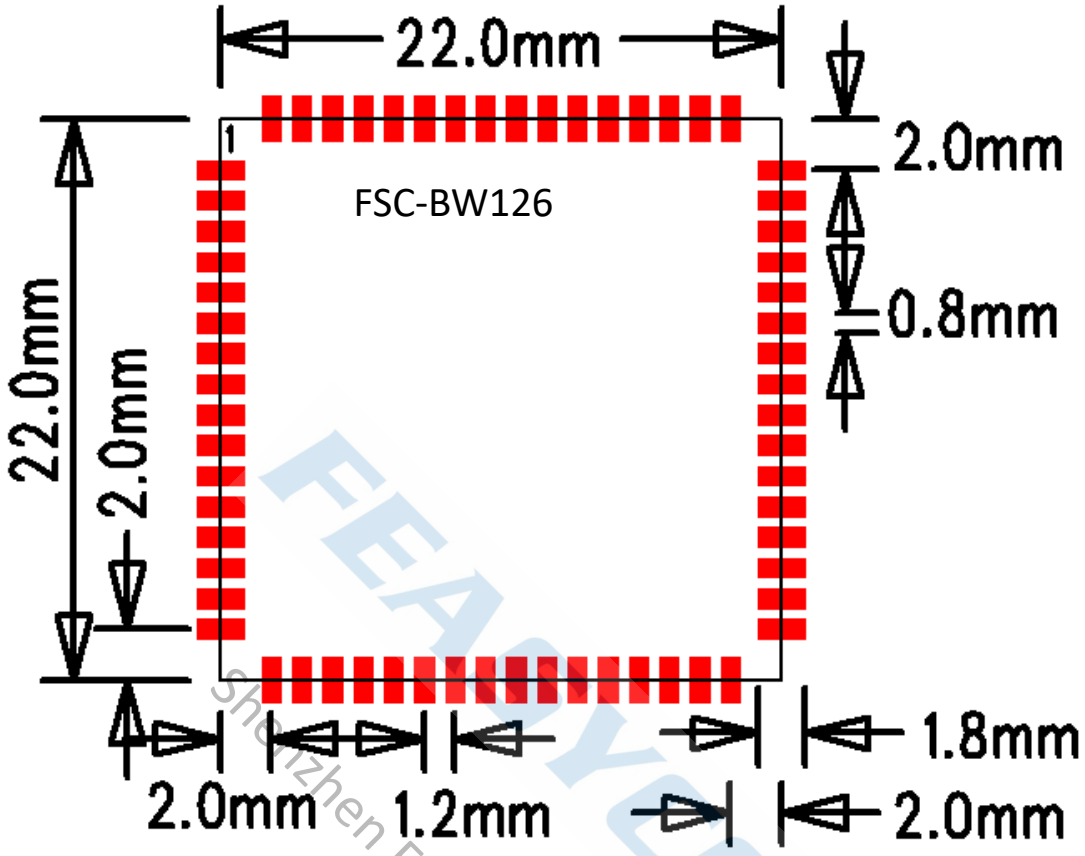


Figure 15: FSC-BW126 footprint Layout Guide (Top View)

9. HARDWARE INTEGRATION SUGGESTIONS

9.1 Requirement for the 3.3V power supply

- To use a dedicated power supply circuit for Wi-Fi (and BT).
- <0.05% line regulation and <0.5%/A load regulation are required for ripple frequency below 100KHz.
- Transient-response: 1, the ripple raised from 100/800mA step-response test should be small than 200mVpp.
  2, The ripple swing shall settle down within 1~2 cycles, 2 cycles for the worst case.
- Power supply spur: make sure the spurs from switching mode power supply or other noisy circuits are reasonably small. Once issue concerned with such a power supply spur, alternative power supply filtering might be needed.
- VBAT: 3.0 to 3.6V (Peak Current2A); VDDIO: 1.7 to 3.6V

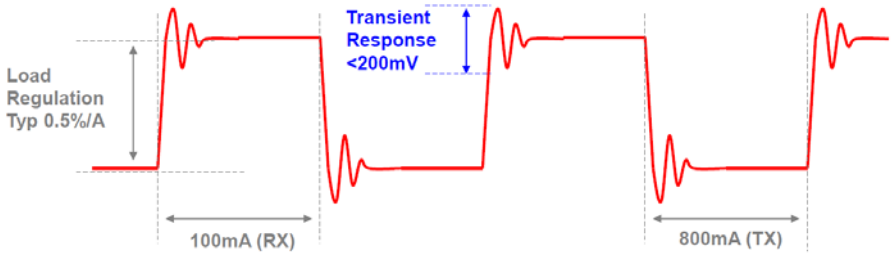


Figure 16: Requirement for the 3.3V power supply

9.2 Connections when BT's HCI is by UART

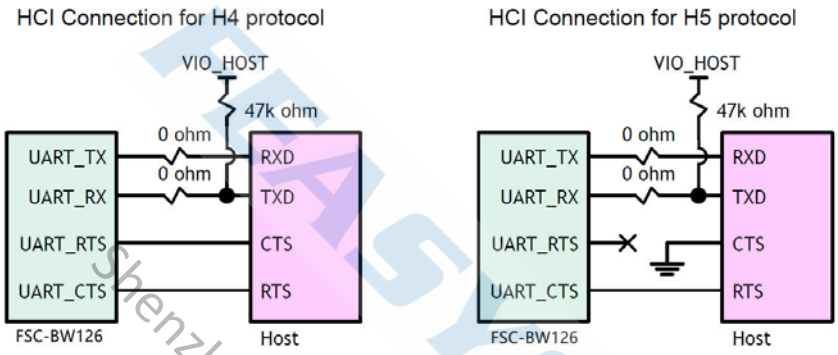


Figure 17: Connections when BT's HCI is by UART

Note:

1. Reserve a 47k pull-high resistor on host TXD when this port is not in output mode for default.

   (If not sure, reserve a 47k resistor is recommended for avoid TXD being floating)

2. There must be 0 ohm jumper-resistors on TX/RX paths, for BQB certification test.

9.3 RF Circuit- RF pads

- Some RF components such as 0402-packaged RLC, connectors, or module pins are with large soldering pad, those pads have higher parasitic capacitance which can impact the characteristic impedance of RF traces.
- The GND under those pads shall be dug out, shown as below, for keeping good 50Ω matching.
- The dig-out layers and area should be calculated carefully, we recommend digging the area a little higher than the simulation results.

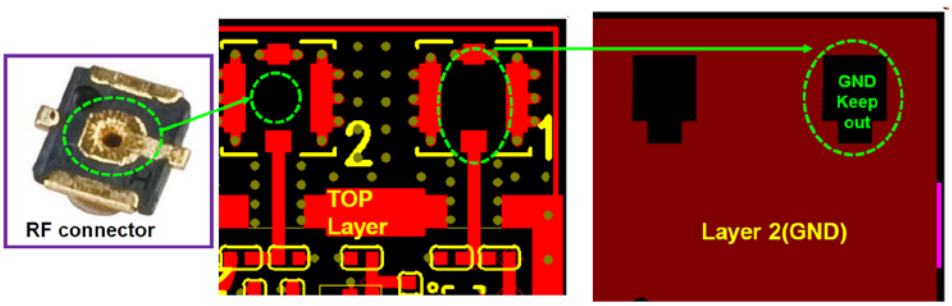


Figure 18: RF Circuit- RF pads

9.4 Soldering Recommendations

FSC-BW126 is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

9.5 Layout Guidelines(Internal Antenna)

Important Note: The antenna of FSC-BW126 needs to support both 2.4GHz and 5.8GHz dual frequency bands. We recommend using external FPC dual-band antennas instead of PCB onboard antennas. The following are general in structions for PCB onboard antennas for reference only.

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.

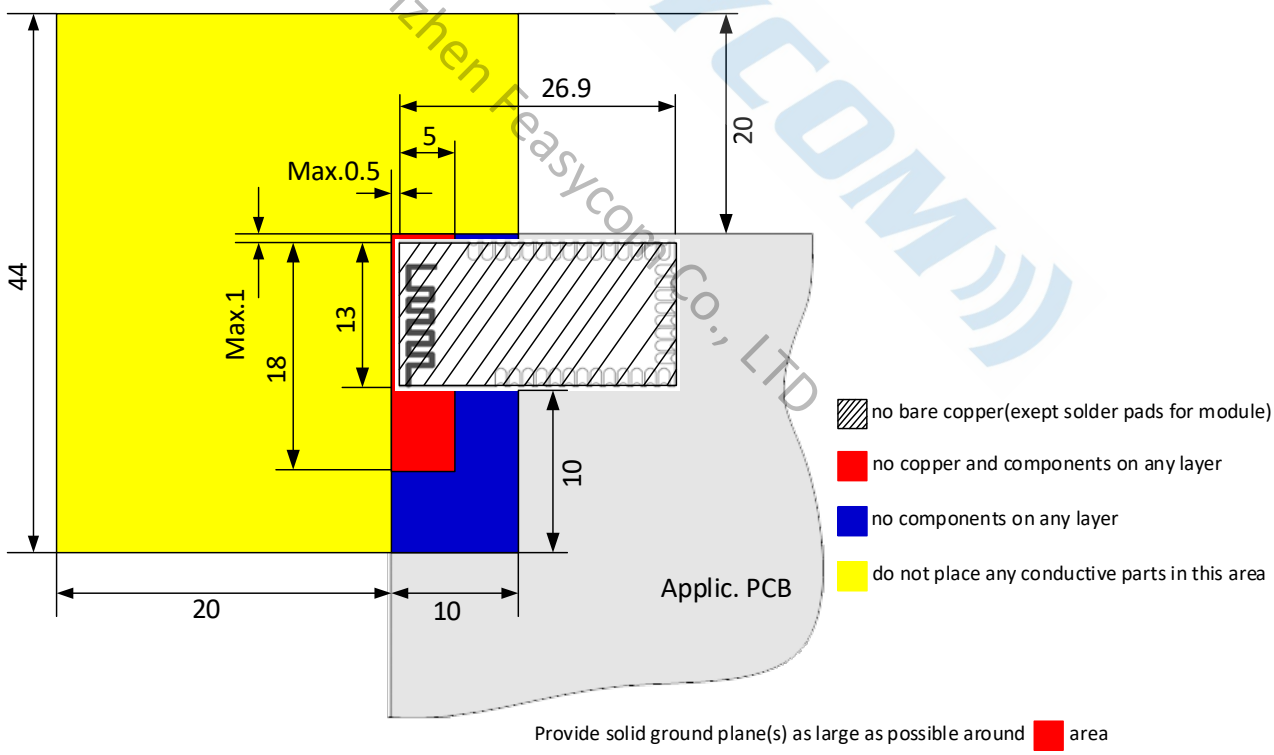


Figure 19: Restricted Area (Reference design) Unit: mm

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

9.6 Layout Guidelines(External Antenna)

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

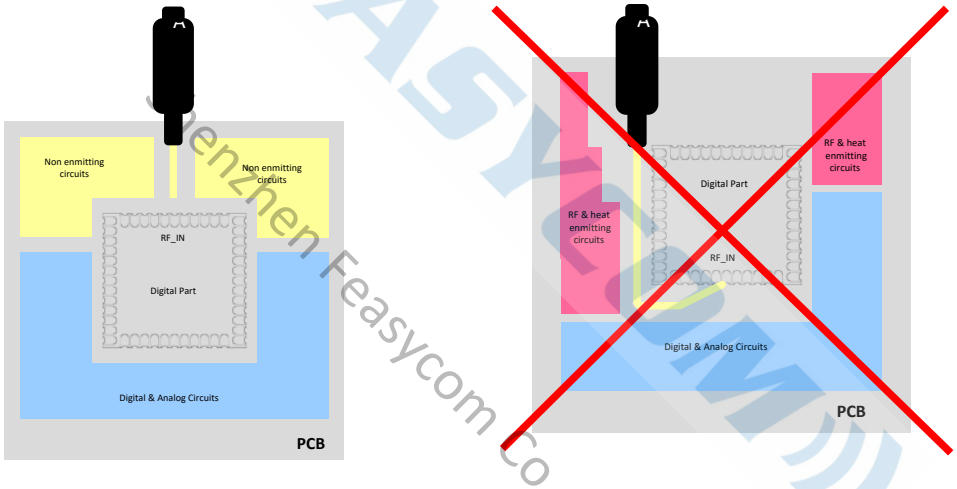


Figure 20: Placement the Module on a System Board

9.6.1 Antenna Connection and Grounding Plane Design

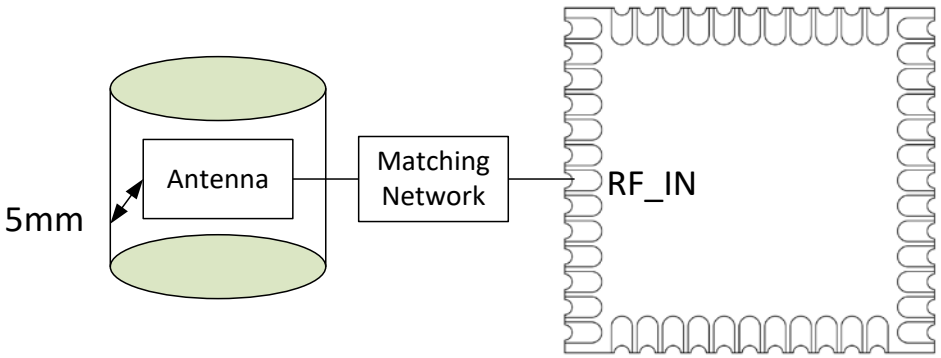


Figure 21: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

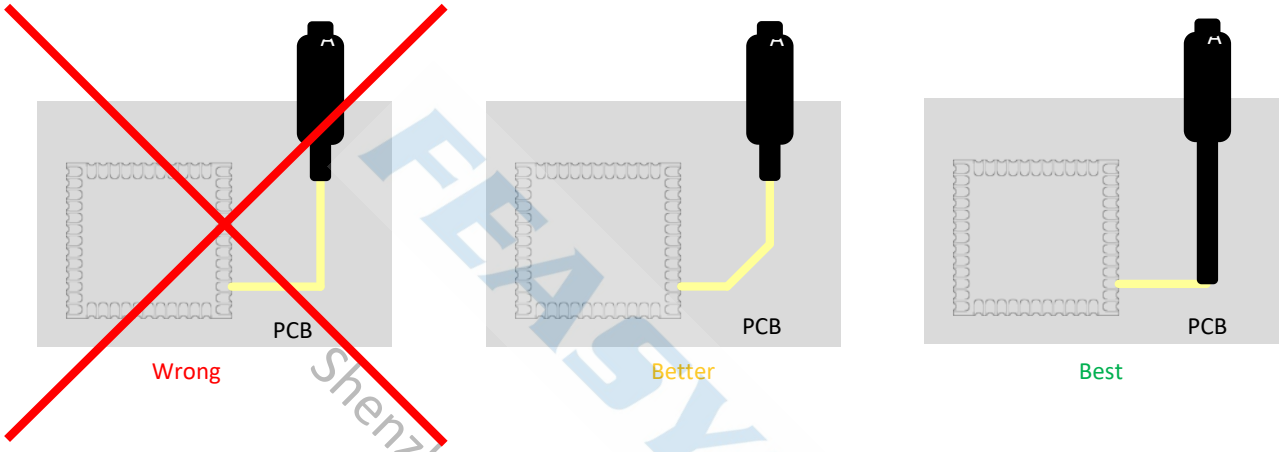


Figure 22: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

10. PRODUCT PACKAGING INFORMATION

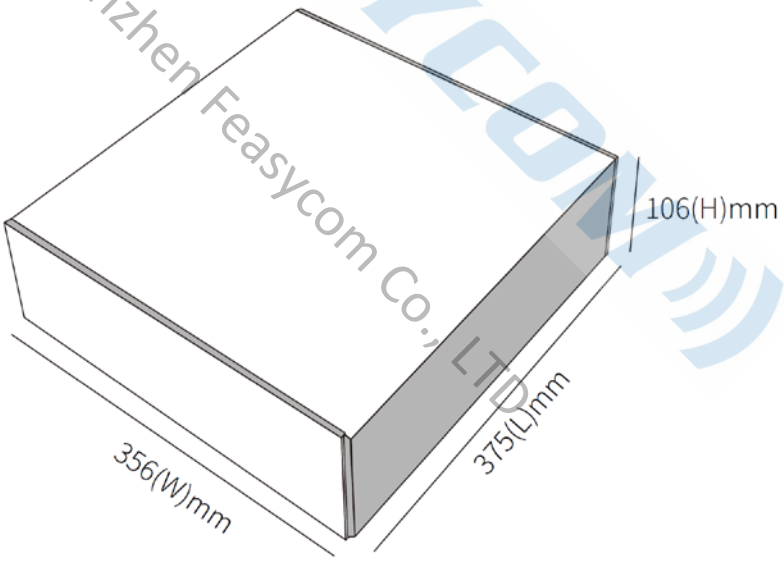
10.1 Default Packing

a, Tray vacuum

b, Tray Dimension: 165mm * 315mm

Figure 23: Tray vacuum

10.2 Packing box (Optional)



* If other packing is required, please confirm with the customer

* Packing: 500pcs per carton (Minimum packing quantity)

* **The outer packing size is for reference only, please refer to the actual size**

Figure 24: Packing Box

11. APPLICATION SCHEMATIC