FSC-BT966

5.0 Dual Mode Bluetooth Module Datasheet

Version 1.4

Revision History

Version	Data	Notes	
1.0	2020/04/11	Initial Version	Fish
1.1	2020/06/01	Add codec chip	Devin Wan
1.2	2020/06/11	Description Update	Devin Wan
1.3	2021/02/19	Update Features description and module pictures	Fish
1.4	2021/03/22	Update chip model	Fish

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1. INTRODUCTION

Overview

FSC-BT966 is a Bluetooth 5.0 dual-mode module which is based on Bluetooth chip CP008,it. It provides a Bluetooth BR/EDR and LE fully compliant system for audio and data communication.

FSC-BT966 integrates an application processor with embedded flash memory, a high-performance stereo codec, a power management subsystem, I2S, SPI, LED drivers, PWM, and ADC in a SoC IC. The dual-core architecture with flash memory enables manufacturers to easily differentiate their products with new features without extending development cycles.

By default, FSC-BT966 module is equipped with powerful and easy-to-use Feasycom firmware. It's easy-to-use and completely encapsulated. Feasycom firmware enables users to access Bluetooth functionality with simple AT commands delivered to the module over serial interface - it's just like a Bluetooth modem.

Therefore, FSC-BT966 provides an ideal solution for developers who want to integrate Bluetooth wireless technology into their design.

Features

- Complies with Bluetooth Core Specification version 5.0 including BR/EDR/BLE
- Support HFP/HSP, A2DP, AVRCP, PBAP, MAP, SPP, GATT profiles
- Broadcom proprietary LE data rate up to 2 Mbps
- BLE HID profile version 1.00 compliant
- Bluetooth Device ID profile version 1.3 compliant
- Supports Generic Access Profile (GAP)
- Supports Adaptive Frequency Hopping (AFH)
- Excellent receiver sensitivity
- Integrated ARM Cortex-M3 microprocessor core
- On-chip power-on reset (POR)
- Integrated low dropout regulators (LDO)
- PCM/I2S Interface
- I2C interface (compatible with NXP I2C slaves)
- RoHS compliant
- Ambient temperature of operation -30°C to +85°C

Application

- Bluetooth speakers
- Home automation
- Point-of-sale input devices
- Blood pressure monitors
- "Find me" devices
- Heart rate monitors
- Thermometers

Module picture as below showing

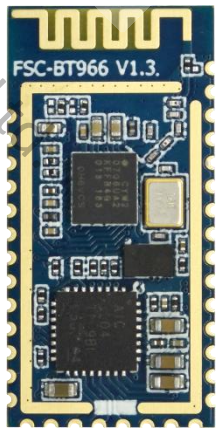


Figure 1: FSC-BT966 Picture

2. General Specification

Table 1: General Specifications

Categories	Features	Implementation
Wireless Specification	On-board chip	CP008
	Bluetooth Version	Bluetooth V5.0 Dual-mode
	Frequency	2.402 - 2.480 GHz
	Transmit Power	+12 dBm (Maximum)
	Receive Sensitivity	-93.5 dBm (Typical)
	Raw Data Rates (Air)	3 Mbps (Classic BT - BR/EDR)
	Modulation	GFSK, π/4-DQPSK, 8-DPSK
Host Interface and Peripherals	UART Interface	TX, RX, CTS, RTS
		General Purpose I/O
		Default 115200,N,8,1
		Baudrate support from 1200 to 921600
		5,6,7,8 data bit character
	GPIO	6 (maximum – configurable) lines
		O/P drive strength (8 mA at 3.3V)
		All of these GPIOs can be configured as ADC inputs
	I^2C Interface	Up to 400 kbps Master I^2C interface
Supply Voltage	Supply	VDD: 3.0 ~ 3.6V
Physical	Dimensions	13mm(W) X 26.9mm(L) X 2.0mm(H); Pad Pitch 1mm
Environmental	Operating	-30°C to +85°C
	Storage	-40°C to +105°C
Miscellaneous	Lead Free	Lead-free and RoHS compliant
	Warranty	One Year
Humidity		10% ~ 90% non-condensing
MSL grade:		MSL 3
ESD grade:		Human Body Model: Class 2 2kV (all pins)
		Charged Device Model: Class III 500 V (all pins)

3. HARDWARE SPECIFICATION

3.1 Block Diagram and PIN Diagram

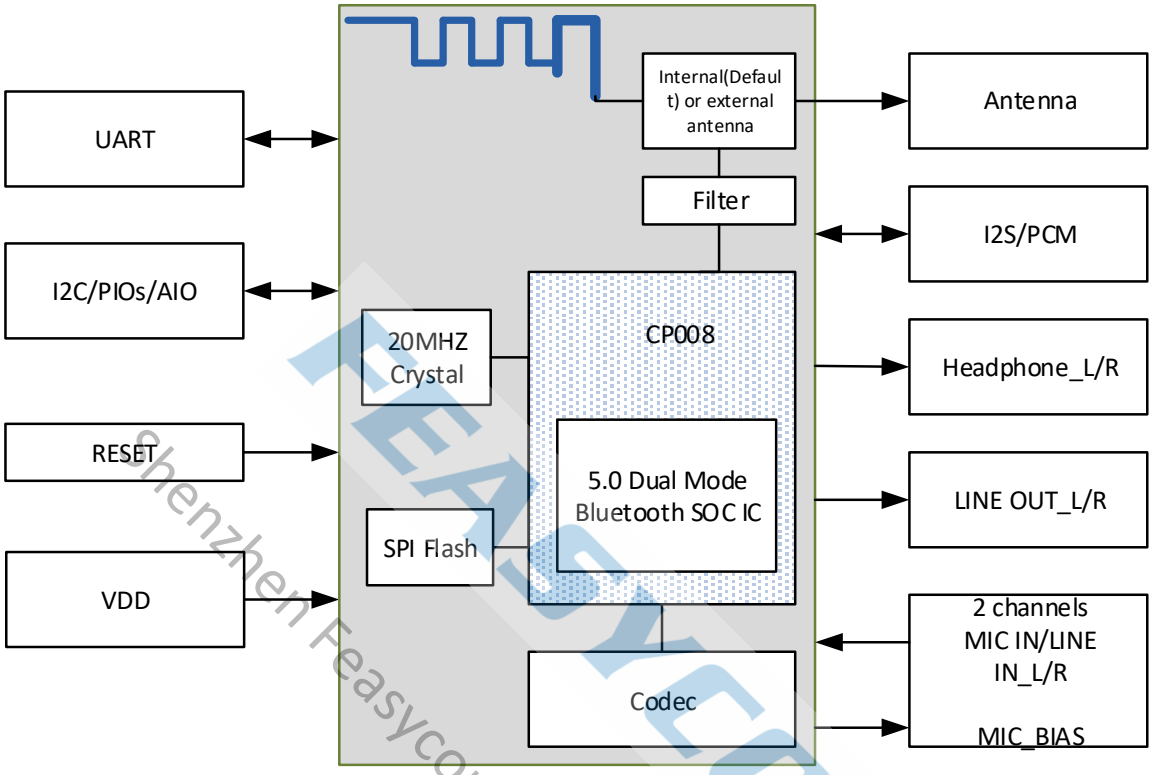


Figure 2: Block Diagram

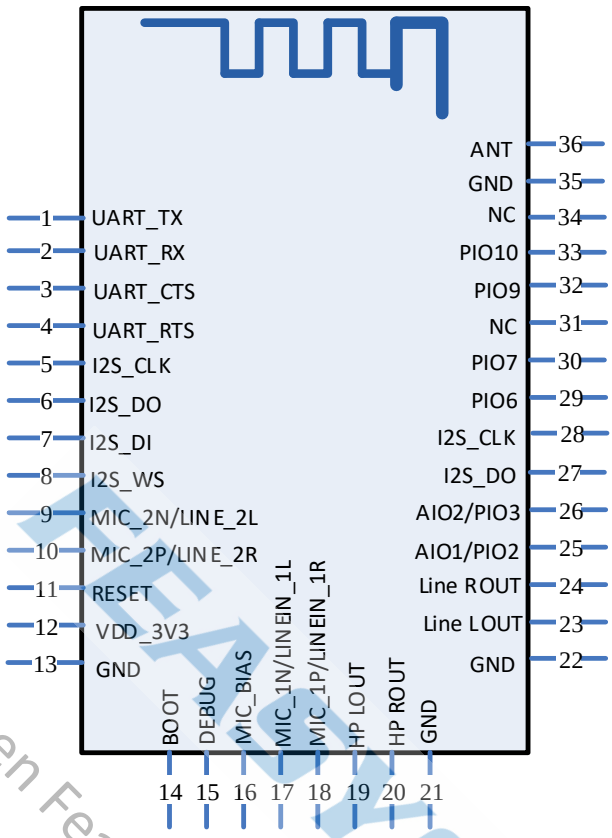


Figure 3: FSC-BT966 PIN Diagram (Top View)

3.2 PIN Definition Descriptions

Table 2: Pin definition

Pin	Pin Name	Type	Pin Descriptions	Notes
1	UART_TX	O	UART Data output Alternative Function: Debug TX	
2	UART_RX	I	UART Data input Alternative Function: Debug RX	
3	UART_CTS	I/O	UART Clear to Send, active low	
4	UART_RTS	I/O	UART Request to Send, active low	
5,28	I2S_CLK	I/O	I2S clock	
6,27	I2S_DO	O	I2S synchronous data output	
7	I2S_DI	I	I2S synchronous data input	
8	I2S_WS	I/O	I2S word select	
9	MIC_2N/LINEIN_2L	I	Multifunction Analog Input, or Single-ended configuration: MIC 2 or Line 2 left or Differential configuration: MIC 2 negative	
10	MIC_2P/LINEIN_2R	I	Multifunction Analog Input, or Single-ended configuration: MIC 2 or Line 2 right or Differential configuration: MIC 2 positive	

11	RESET	I	Active-low reset input
12	VDD_3V3	I/O	Power supply voltage 3.0V~ 3.6V
13	GND	Vss	Power Ground
14	BOOT	I	NC (Do not connect to any pin)
15	DEBUG	I	NC (Do not connect to any pin)
16	MIC_BIAS	O	Microphone bias voltage output
17	MIC_1N/LINEIN_1L	I	Multifunction Analog Input, or Single-ended configuration: MIC 1 or Line 1 left or Differential configuration: MIC 1 negative
18	MIC_1P/LINEIN_1R	I	Multifunction Analog Input, or Single-ended configuration: MIC 1 or Line 1 right or Differential configuration: MIC 1 positive
19	HP LOUT	O	Left high power output driver
20	HP ROUT	O	Right high power output driver
21	GND	Vss	Power Ground
22	GND	Vss	Power Ground
23	Line LOUT	O	Left line output
24	Line ROUT	O	Right line output
25	AIO1/PIO2	I/O	Analogue I/O Alternative Function: Programmable input/output
26	AIO2/PIO3	I/O	Analogue I/O Alternative Function: Programmable input/output
29	PIO6	I/O	Programmable input/output Alternative Function: I^2C Serial Clock input/output
30	PIO7	I/O	Programmable input/output Alternative Function:I^2C Serial Data input/output
31	NC		NC (Do not connect to any pin)
32	PIO9	I/O	LED indication, output Alternative Function: Programmable input/output
33	PIO10	I/O	Connection state, output. H=Connect , L=No connection Alternative Function: Programmable input/output
34	NC		NC (Do not connect to any pin)
35	GND	Vss	Power Ground
36	ANT	O	RF output

4. PHYSICAL INTERFACE

4.1 Power Management

The transient response of the regulator is important. If the power rails of the module are supplied from an external voltage source, the transient response of any regulator used should be 20μs or less. It is essential that the power rail recovers quickly.

4.2 Reset

An external active-low reset signal, RESET_N, can be used to put the FSC-BT966 in the reset state. An external voltage detector reset IC with 50 ms delay is needed on the RESET_N. The RESET_N should be released only after the VDDO supply voltage level has been stabilized for 50 ms.

4.3 General Purpose Analog IO

FSC-BT966 has 2 general-purpose analogue interface pins, AIO1, AIO2.

4.4 General Purpose Digital IO

FSC-BT966 provides up to 6 lines of programmable bidirectional I/O.

4.5 RF Interface

For this module, the antenna must be connected to work properly.

The user can connect a 50ohm antenna directly to the RF port.

- 2402–2480 MHz Bluetooth 5.0 Dual Mode (BT and BLE); 1 Mbps to 3 Mbps over the air data rate.
- TX output power of: Class1: +12dBm(MAX)@GFSK Tx power
  Class1: +9dBm(MAX)@EDR Tx power
  Class 2: +2dBm(MAX)@GFSK Tx power

- Receiver to achieve maximum sensitivity: -93.5dBm @ GFSK,0.1% BER, 1 Mbps
  -96.5dBm @ LE GFSK, 0.1% BER, 1 Mbps
  -95.5dBm @ π/4-DQPSK, 0.01% BER, 2 Mbps
  -89.5dBm @ 8-DPSK, 0.01% BER, 3 Mbps

4.6 Serial Interfaces

4.6.1 UART Interface

FSC-BT966 provides one full-duplex asynchronous communication channel of Universal Asynchronous Receiver/Transmitters (UART). The UART controller performs a serial-to-parallel conversion on data received from the peripheral and a parallel-to-serial conversion on data transmitted from the CPU. Each UART Controller channel supports ten types of interrupts.

This is a standard UART interface for communicating with other serial devices. The UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

When the module is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators.

This module output is at 3.3V CMOS logic levels (tracks VCC). Level conversion must be added to interface with an RS-232 level compliant interface.

Some serial implementations link CTS and RTS to remove the need for handshaking. We do not recommend linking CTS and RTS except for testing and prototyping. If these pins are linked and the host sends data when the FSC-BT966 deasserts its RTS signal, there is significant risk that internal receive buffers will overflow, which could lead to an internal processor crash. This drops the connection and may require a power cycle to reset the module. We recommend that you adhere to the correct CTS/RTS handshaking protocol for proper operation.

Table 3: Possible UART Settings

Parameter		Possible Values
Baudrate	Minimum	1200 baud (≤2%Error)
	Standard	115200bps(≤1%Error)
	Maximum	4Mbaud(≤1%Error)
Flow control		RTS/CTS, or None
Parity		None, Odd or Even
Number of stop bits		1 /2
Number of data bits		8

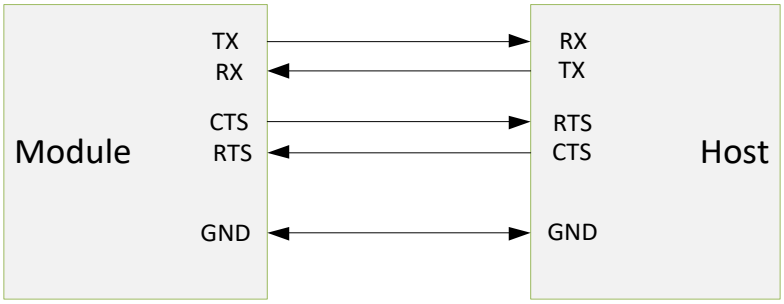


Figure 4: UART Connection

4.6.2 I²C Interface

The FSC-BT966 provides a 2-pin master I2C interface, which can be used to retrieve configuration information from an external EEPROM or to communicate with peripherals such as trackball or touch-pad modules, and motion tracking ICs used in mouse devices. The BSC interface is compatible with I2C slave devices. I2C does not support multimaster capability or flexible wait-state insertion by either master or slave devices.

Data is transferred between a Master and a Slave synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8-bit long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to the following figure for more details about I²C Bus Timing.

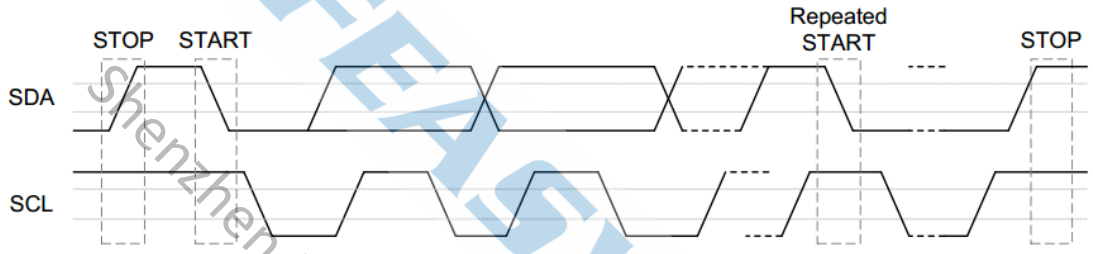


Figure 5: I2C Bus Timing

The device on-chip I²C logic provides the serial interface that meets the I²C bus standard mode specification. The I²C port handles byte transfers autonomously. The I²C H/W interfaces to the I²C bus via two pins: SDA and SCL. Pull up resistor is needed for I²C operation as these are open drain pins. When the I/O pins are used as I²C port, user must set the pins' function to I²C in advance.

4.6.3 I2S interface

FSC-BT966 supports I2S input and output via its two industry-standard I2S digital audio interfaces, left-justified or right-justified.

FSC-BT966 supports several alternative PCM data formats. For further details, contact Feasycom. When in PCM mode, the following pin name to function mappings apply.

Table 4: Alternative functions of the digital audio bus interface on the PCM interface

I2S Pin	PCM function
I2S_DO	PCM_OUT
I2S_DI	PCM_IN
I2S_WS	PCM_SYNC
I2S_CLK	PCM_CLK

5. ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

Absolute maximum ratings for supply voltage and voltages on digital and analogue pins of the module are listed below. Exceeding these values causes permanent damage.

Table 5: Absolute Maximum Rating

Parameter	Min	Max	Unit
Ambient temperature of operation	-30	85	℃
Storage temperature	-40	125	℃
VDD	-0.5	3.6	V

5.2 Recommended Operating Conditions

Table 6: Recommended Operating Conditions

Parameter	Min	Type	Max	Unit
Input supply voltage, Vin	3.0	3.3	3.6	V
Operating Temperature	-30	25	+85	℃
Lout， Rout-- Stereo line output load resistance	0.6	10		kΩ

5.3 Input/output Terminal Characteristics

5.3.1 Audio features

Table 7: DC Characteristics (V_{DD} - V_{SS} = 3 ~ 3.6 V, T_A = 25°C)

Parameter		TEST CONDITIONS	Min	Type	Max	Unit
AUDIO ADC - sine wave input						
Input signal level (0dB)		Single-ended, CM = 0.9V	-	0.5	-	V_{RMS}
Device Setup		1kHz sine wave input Single-ended Configuration R_{in} = 20K, f_s = 48kHz, AOSR = 128, MCLK = 256*f_s, PLL Disabled; AGC = OFF, Channel Gain = 0dB, Processing Block = PRB_R1, Power Tune = PTM_R4				
SNR	Signal-to-noise ratio, A-weighted(1) (2)	Inputs ac-shorted to ground	80	91		dB
DR	Dynamic range A-weighted(1) (2)	–60dB full-scale, 1-kHz input signal		90		dB
THD+N	Total Harmonic Distortion plus Noise	–3 dB full-scale, 1-kHz input signal		-80	-70	dB
AUDIO ADC - Differential Input						
Input signal level (0dB)		Differential Input, CM=0.9V		10		mV

	Device Setup	1kHz sine wave input Differential configuration INL routed to Right ADC INR routed to Left ADC R_{in} =10K, f_s =48kHz, AOSR=128 MCLK = 256* f_s PLL Disabled AGC = OFF, Channel Gain=40dB Processing Block= PRB_R1, Power Tune = PTM_R4		
ICN	Idle-Channel Noise, A-weighted(1) (2)	Inputs ac-shorted to ground, input referred noise	2	uV_{RMS}

AUDIO ADC - Other			
Gain Error	1kHz sine wave input Single-ended configuration R_{in} = 20K fs = 48kHz, AOSR=128, MCLK = 256* f_s, PLL Disabled AGC = OFF, Channel Gain=0dB Processing Block = PRB_R1, Power Tune = PTM_R4, CM=0.9V	–0.02	dB
Input Channel Separation	1kHz sine wave input at -3dBFS Single-ended configuration INL routed to Left ADC INR routed to Right ADC, R_{in} = 20K AGC = OFF, AOSR = 128, Channel Gain=0dB, CM=0.9V	103	dB
Input Pin Crosstalk	1kHz sine wave input at –3dBFS. INL routed to Left ADC INR routed to Right ADC ac-coupled to ground Single-ended configuration R_{in} = 20K, AOSR=128 Channel, Gain=0dB, CM=0.9V	112	dB
PSRR	217Hz, 100mVpp signal on AVdd, Single-ended configuration, R_{in}=20K, Channel Gain=0dB; CM=0.9V	54	dB
ADC programmable gain amplifier gain	Single-Ended, R_{in} = 10K, PGA gain set to 0dB	0	dB
	Single-Ended, R_{in} = 10K, PGA gain set to 47.5dB	47.1	dB
	Single-Ended, R_{in} = 20K, PGA gain set to 0dB	-5	dB
	Single-Ended, R_{in} = 20K, PGA gain set to 47.5dB	41.1	dB
	Single-Ended, R_{in} = 40K, PGA gain set to	-10	dB

	0dB		
	Single-Ended, R_{in} = 40K, PGA gain set to 47.5dB	35.1	dB
ADC programmable gain amplifier step size	1-kHz tone	0.5	dB
ANALOG BYPASS TO LINE-OUT AMPLIFIER, PGA MODE			
Device Setup	Load = 10KΩ (single-ended), 56pF; Input and Output CM=0.9V; LINE Output on LDOIN Supply; INL routed to ADCPGA_L and INR routed to ADCPGA_R; R_{in} = 20k ADCPGA_L routed to LOL and ADCPGA_R routed to LOR; Channel Gain = 0dB		
Gain Error		0.6	dB
Noise, A-weighted(1)	Idle Channel, INL and INR ac-shorted to ground	7	uV_{RMS}
	Channel Gain=40dB, Input Signal (0dB) = 5mV_{rms} Inputs ac-shorted to ground, Input Referred	3.4	uV_{RMS}
MICROPHONE BIAS			
Bias voltage	Bias voltage CM=0.9V, LDOin = 3.3V Micbias Mode 3, Connect to AVdd	AVdd	V
	CM=0.75V, LDOin = 3.3V Micbias Mode 3, Connect to AVdd	AVdd	V
Output Noise	CM=0.9V, Micbias Mode 2, A-weighted, 20Hz to 20kHz bandwidth, Current load = 0mA.	10	uV_{RMS}
Current Sourcing	Micbias Mode 3, Connect to AVdd	3	mA
Inline Resistance	Micbias Mode 3, Connect to AVdd	140	Ω
AUDIO DAC – STEREO SINGLE-ENDED LINE OUTPUT 1			
Device Setup	Load = 10 kΩ (single-ended), 56pF Line Output on AVdd Supply Input & Output CM=0.9V DOSR = 128, MCLK=256* fs, Channel Gain = 0dB, word length = 16 bits, Processing Block = PRB_P1, Power Tune = PTM_P3		
Full scale output voltage (0dB)		0.5	V_{RMS}

SNR	Signal-to-noise ratio A-weighted(1) (2)	All zeros fed to DAC input	87	98		dB
DR	Dynamic range, A-weighted (1) (2)	–60dB 1kHz input full-scale signal, Word length=20bits		100		dB
THD+N	Total Harmonic Distortion plus Noise	–3dB full-scale, 1-kHz input signal		-81	-68	dB
	DAC Gain Error	0 dB, 1kHz input full scale signal		0.4		dB
	DAC Mute Attenuation	Mute		117		dB
	DAC channel separation	–1 dB, 1kHz signal, between left and right HP out		110		dB
	DAC PSRR	100mVpp, 1kHz signal applied to AVdd		72		dB
		100mVpp, 217Hz signal applied to AVdd		75		dB
						dB
AUDIO DAC – STEREO SINGLE-ENDED LINE OUTPUT 2						
	Device Setup	Load = 10 kΩ (single-ended), 56pF Line Output on AVdd Supply Input & Output CM=0.75V; AVdd=1.5V DOSR = 128, MCLK=256* fs, Channel Gain = -2dB, word length = 20bits, Processing Block = PRB_P1, Power Tune = PTM_P4				
	Full scale output voltage (0dB)			0.355		V_{RMS}
SNR	Signal-to-noise ratio A-weighted(1) (2)	All zeros fed to DAC input		97		dB
DR	Dynamic range, A-weighted (1) (2)	–60dB 1kHz input full-scale signal,		96		dB
THD+N	Total Harmonic Distortion plus Noise	–1dB full-scale, 1-kHz input signal		-82		dB
AUDIO DAC – STEREO SINGLE-ENDED HEADPHONE OUTPUT 1						
	Device Setup	Load = 16Ω (single-ended), 50pF Headphone Output on AVdd Supply, Input & Output CM=0.9V, DOSR = 128, MCLK=256* fs, Channel Gain=0dB word length = 16 bits; Processing Block = PRB_P1 Power Tune = PTM_P3				
	Full scale output voltage (0dB)			0.5		V_{RMS}
SNR	Signal-to-noise ratio A-weighted(1) (2)	All zeros fed to DAC input	85	98		dB
DR	Dynamic range, A-weighted (1) (2)	–60dB 1kHz input full-scale signal, Word Length =20 bits, Power Tune = PTM_P4		97		dB
THD+N	Total Harmonic Distortion plus Noise	–3dB full-scale, 1-kHz input signal		-81	-68	dB
	DAC Gain Error	0dB, 1kHz input full scale signal		–0.3		dB
	DAC Mute Attenuation	Mute		120		dB
	DAC channel separation	–1dB, 1kHz signal, between left and right HP out		108		dB

DAC PSRR	100mVpp, 1kHz signal applied to AVdd	71	dB
	100mVpp, 217Hz signal applied to AVdd	76	dB
Power Delivered	R_L=16Ω, Output Stage on AVdd = 1.8V THDN < 1%, Input CM=0.9V, Output CM=0.9V	15	mW
	R_L=16Ω Output Stage on LDOIN = 3.3V, THDN < 1% Input CM=0.9V, Output CM=1.65V	64	mW
AUDIO DAC – STEREO SINGLE-ENDED HEADPHONE OUTPUT 1			
Device Setup	Load = 16W (single-ended), 50pF, Headphone Output on AVdd Supply, Input & Output CM=0.75V; AVdd=1.5V,DOSR = 128, MCLK=256* fs, Channel Gain = –2dB, word length=20-bits; Processing Block = PRB_P1, Power Tune = PTM_P4		
Full scale output voltage (0dB)		0.375	V_{RMS}
SNR Signal-to-noise ratio A-weighted (1) (2)	All zeros fed to DAC input	97	dB
DR Dynamic range, A-weighted (1) (2)	–60dB 1kHz input full-scale signal,	96	dB
THD+N Total Harmonic Distortion plus Noise	–1dB full-scale, 1-kHz input signal	-81	dB

(1) Ratio of output level with 1-kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.

(2) All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values

5.3.2 Digital I/O Characteristics

Table 8: At 25° C, AVdd = 3.3V,fs (Audio) = 48kHz, Cref = 10 mF on REF PIN,PLL disabled unless otherwise noted.

Parameter	Min	Type	Max	Unit
Input Voltage				
V_{IL} - Standard IO Low level input voltage	-	-	0.8	V
V_{IH} - Standard IO Low level input voltage	2.0	-	-	V
Output Voltage				
V_{OL} - Low Level Output Voltage	-	-	0.4	V
V_{OH} - High Level Output Voltage		-	-	V
Tr/Tf	-	-	5	nS

Input Currents				
Low	-	-	-1.0	uA
High	-	-	-1.0	uA
Output Currents				
Low	-	-	-2.0	mA
High	-	-	-4.0	mA

5.4 Current Consumptions

Table 9: Bluetooth, BLE, BR and EDR Current Consumption, Class 1

Mode	Remarks	Type	Unit
3DH5/3DH5	-	37.10	mA
BLE			
BLE	Connected 600 ms interval	211	uA
BLE ADV	1.00 sec ADV interval	176	uA
BLE Scan	No devices present. A 1.28-sec interval with 11.25 ms scan window.	355	uA
DMx/DHx			
DM1/DH1	-	32.15	mA
DM3/DH3	-	38.14	mA
DM5/DH5	-	38.46	mA
HIDOFF	Deep sleep	2.69	uA
Page scan	Periodic scan rate is 1.28 sec	0.486	mA
Receive			
1Mbps	Peak current level during reception of a basic-rate packet.	26.373	mA
EDR	Peak current level during the reception of a 2 or 3 Mbps rate packet.	26.373	mA
Sniff Slave			
11.25ms	-	4.95	mA
22.5ms	-	2.6	mA
495.00ms	Based on one attempt and no timeout.	254	uA
Transmit			
1Mbps	Peak current level during the transmission of a basic-rate packet: GFSK output power = 10 dBm.	60.289	mA
EDR	Peak current level during the transmission of a 2 or 3 Mbps rate packet. EDR output power = 8 dBm.	52.485	mA

6. MSL &ESD Protection

Table 10: MSL and ESD

Parameter	Class	Max Rating
MSL grade(with JEDEC J-STD-020)		MSL 3
Human Body Model Contact Discharge per ANSI/ESDA/JEDEC JS-001	2	2kV(all pins)
Charged Device Model Contact Discharge per JEDEC/EIA JESD22-C101	III	500V (all pins)

7. RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccate (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the below **Table 11** and follow instructions specified by IPC/JEDEC J-STD-033.

Note: The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the below **Table 11**, the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccate and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60%RH.

Table 11:Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated@ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Feasycom surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

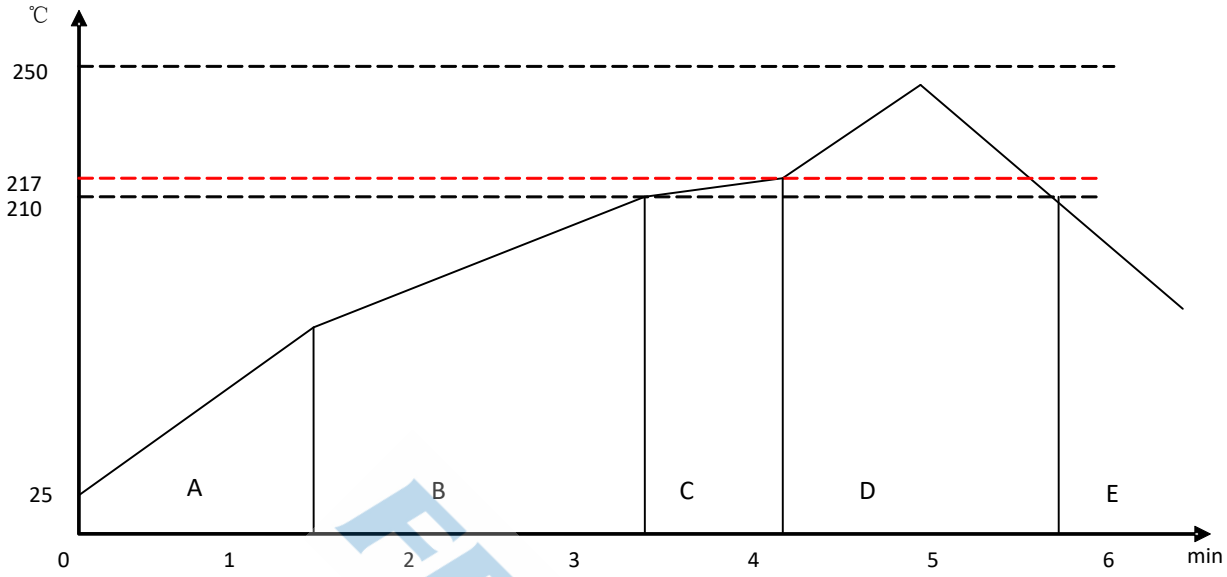


Figure 6: Typical Lead-free Re-flow

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

Equilibrium Zone 2 (C) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

8. MECHANICAL DETAILS

8.1 Mechanical Details

- Dimension: 13mm(W) x 26.9mm(L) x 2.0mm(H) Tolerance: ±0.1mm
- Module size: 13mm X 26.9mm Tolerance: ±0.2mm
- Pad size: 1mmX0.8mm Tolerance: ±0.2mm
- Pad pitch: 1.5mm Tolerance: ±0.1mm

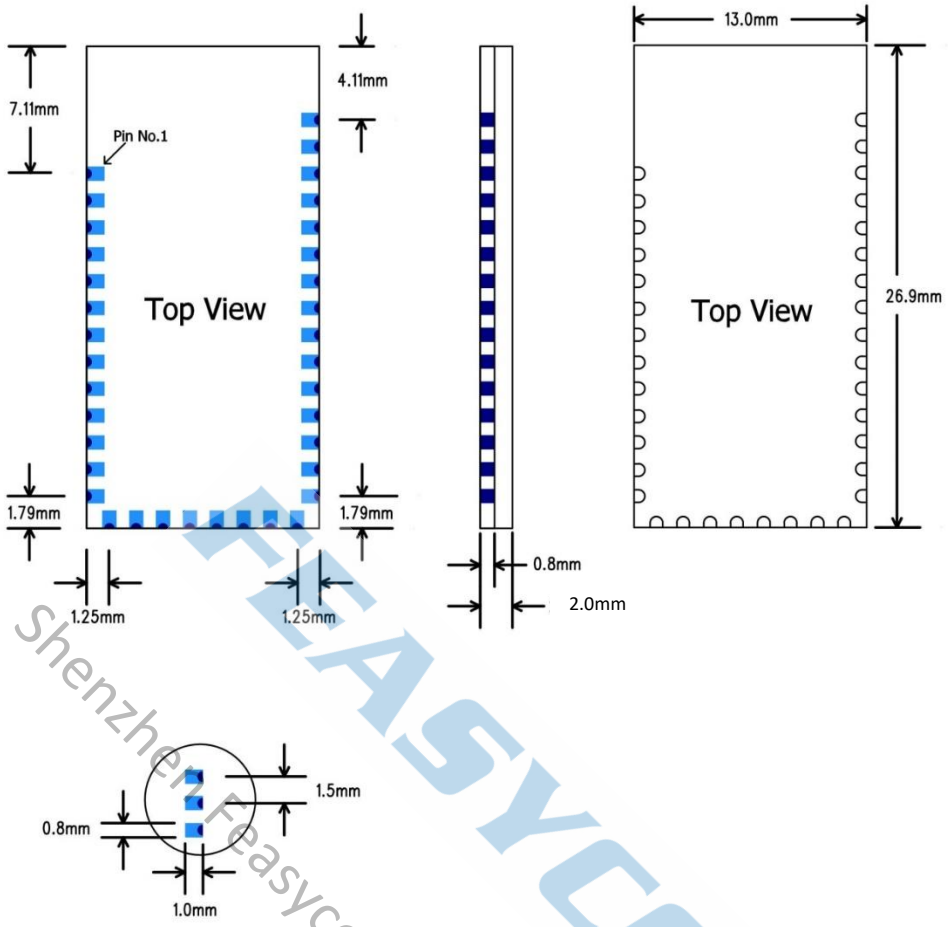


Figure 7: FSC-BT966 footprint

9. HARDWARE INTEGRATION SUGGESTIONS

9.1 Soldering Recommendations

FSC-BT966 is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

9.2 Layout Guidelines(Internal Antenna)

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.

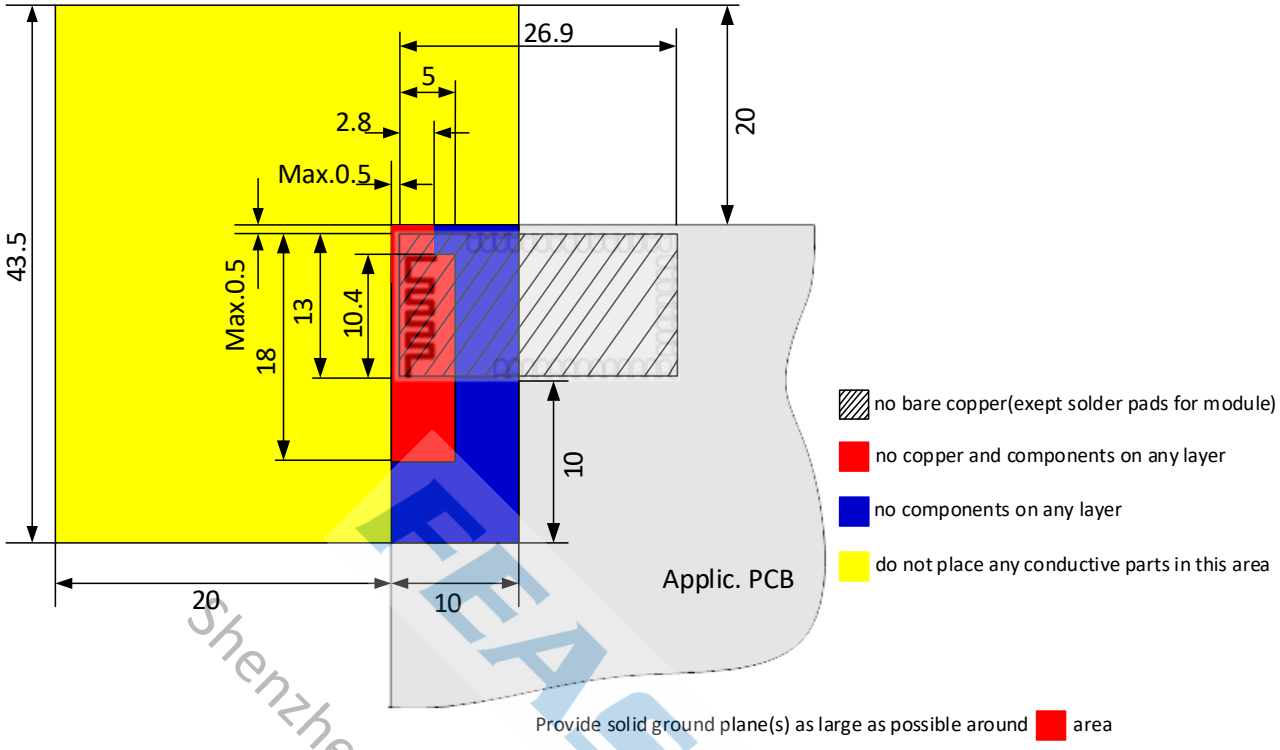


Figure 8: Restricted Area （Unit：mm）

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

9.3 Layout Guidelines(External Antenna)

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in **Figure** below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

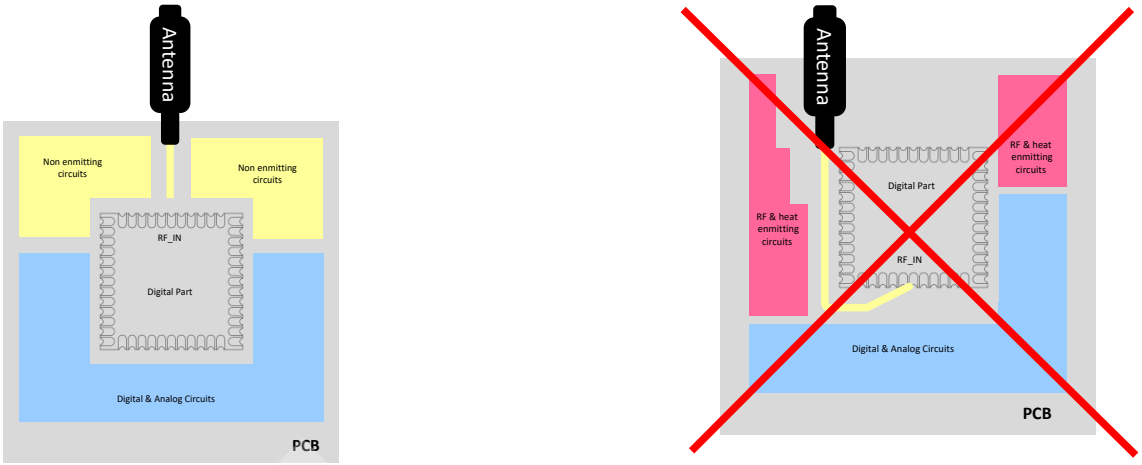


Figure 9: Placement the Module on a System Board

9.3.1 Antenna Connection and Grounding Plane Design

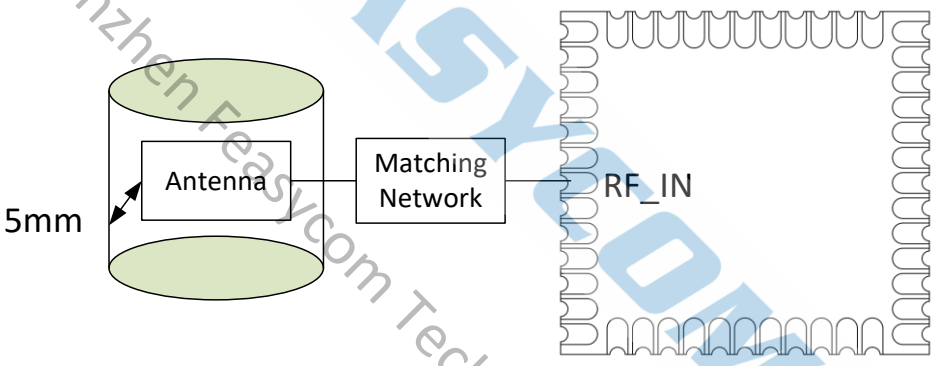


Figure 10: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

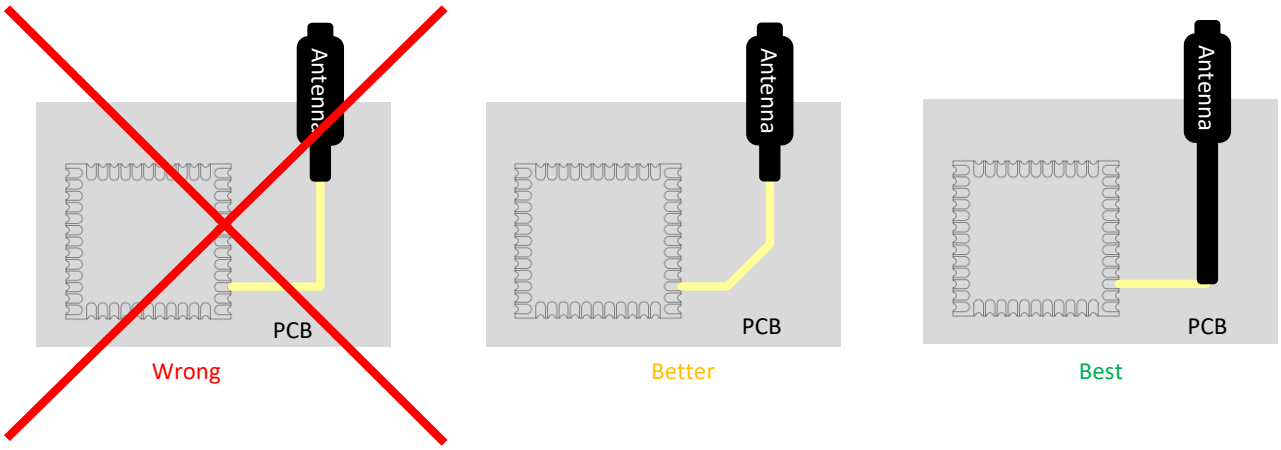


Figure 11: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

10. PRODUCT PACKAGING INFORMATION

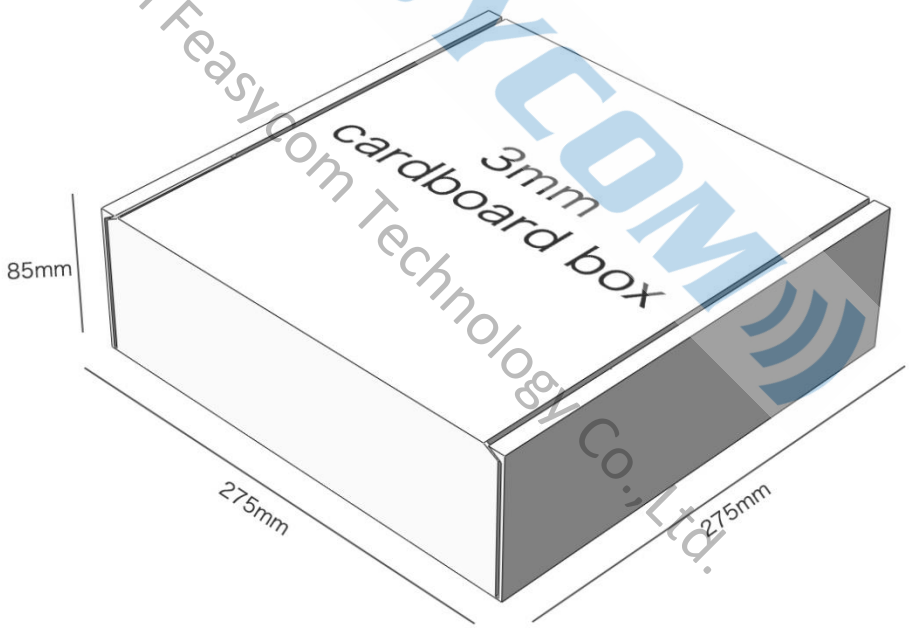
10.1 DefaultPacking

a, Tray vacuum

b, Tray Dimension: 180mm * 195mm

Figure 12: Tray vacuum

10.2 Packing box(Optional)



* If require any other packing, must be confirmed with customer

* Package: 2000PCS Per Carton (Min Carton Package)

Figure 13: Packing Box

11. APPLICATION SCHEMATIC