FSC-BT982

5.2 Dual Mode Bluetooth Module

Version 1.4

Revision History

Version	Data	Notes	
1.0	2023/04/23	Initial Version	Devin Wan
1.1	2021/06/08	Update transmit power	Fish
1.2	2021/07/30	Update physical images	Origami
1.3	2022/10/13	Update the description of the bug	Marsh
1.4	2022/11/28	Update storage temperature: -20 C° to +85C°	Marsh

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1. INTRODUCTION

Overview

FSC-BT982 is a high-performance, highly integrated Bluetooth 5.2 BR/EDR/BLE, designed to operate on the 2400MHz to 2480Mhz ISM frequency band.

Abundant peripherals, power-on reset (POR), arithmetic accelerators further reduce the cost and size of the entire system.

By default, Feasycom standard firmware is built-in, and customized firmware is also available.FSC-BT982 is a suitable product for designers who want to add wireless functions to their products.

Features

- Bluetooth 5.2 Classical/BLE Proprietary double-mode RF SOC
- UART programming and data interface (baudrate can up to 921600bps)
- Digital Peripherals
  - LED drive capability
  - AES256 HW encryption
- Dual Core Digital Architecture
  - ARM Cortex-M0 Core for application
  - CPU clock speed up to 192Mhz
- 2.4GHz Transceiver
  - Single-end RFIO
  - -95dBm in BLE mode
  - Support 250kbps, 1/2/3 Mbps data rates
  - Tx Power 0dBm
- Postage stamp sized form factor
- Working current is 5mA
- Support External Antenna
- RoHS compliant

Application

- Health Thermometer
- Heart Rate
- Blood Pressure
- Proximity

Module picture as below showing

Figure 1: FSC-BT982 Picture

2. General Specification

Table 1: General Specifications

Categories	Features	Implementation
Wireless Specification	Bluetooth Version	Bluetooth v5.2 Dual mode
	Frequency	2.400 - 2.480 GHz
	Transmit Power	0dBm
	Receive Sensitivity	-95 dBm@0.1%BER (BLE mode)
	Modulation	GFSK, π/4 DQPSK, 8DPSK
	Raw Data Rates (Air)	3 Mbps
Host Interface and Peripherals	UART Interface	TX, RX, Supports Automatic Flow Control (CTS and RTS lines).
		General Purpose I/O
		Default 115200,N,8,1
		Baudrate support from 1200 to 921600
		5, 6, 7, 8 data bit character
	GPIO	6 (maximum – configurable) lines
Profiles	Classic Bluetooth	Support
	Bluetooth Low Energy	Support
Maximum Connections	Classic Bluetooth	1 Clients
	Bluetooth Low Energy	1 Clients
FW upgrade		Jlink
Supply Voltage	Supply	3.3V
Power Consumption		Working current 5mA
Physical	Dimensions	16.55mm X 10.88mm X 2.2mm;
Environmental	Operating	-10°C to +85°C
	Storage	-20°C to +85°C
Miscellaneous	Lead Free	Lead-free and RoHS compliant
	Warranty	One Year
Humidity		10% ~ 90% non-condensing
MSL grade:		MSL 3
ESD grade:		Human Body Model: Class-2 Machine Model: Class-B

3. HARDWARE SPECIFICATION

3.1 Block Diagram and PIN Diagram

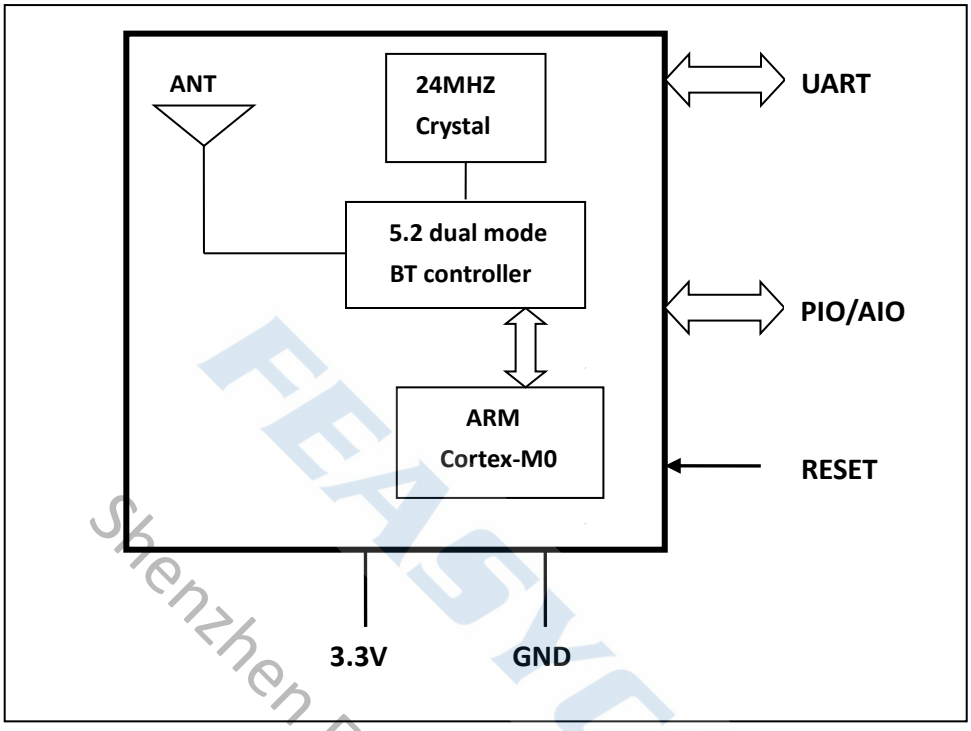


Figure 2: Block Diagram

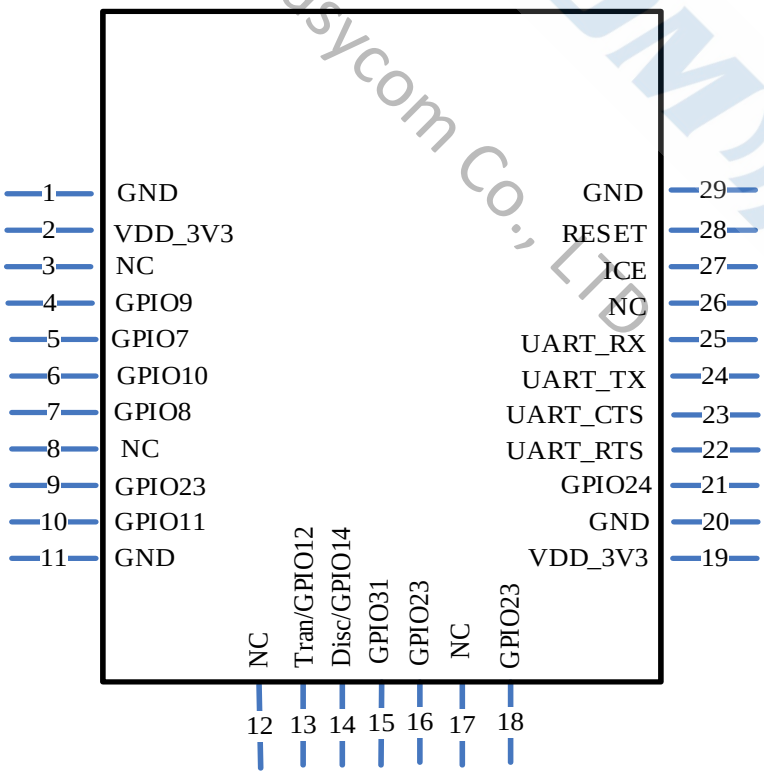


Figure 3: FSC-BT982 PIN Diagram(Top View)

3.2 PIN Definition Descriptions

Table 2: Pin definition

Pin	Pin Name	Type	Pin Descriptions
1	GND	Vss	Power Ground
2	VDD_3V3	Vdd	Power supply voltage 3.3V
3	NC		
4	GPIO0	I/O	Programmable input/output line
5	GPIO1	I/O	Programmable input/output line
6	GPIO2	I/O	Programmable input/output line
7	GPIO3	I/O	Programmable input/output line
8	NC		
9	GPIO4	I/O	Programmable input/output line
10	GPIO5	I/O	Programmable input/output line
11	GND	Vss	Power Ground
12	NC		
13	Tran/GPIO6	I/O	Programmable input/output line Alternative Function : Host MCU change UART transmission mode
14	Disc/GPIO7	I/O	Programmable input/output line Alternative Function : Host MCU disconnect bluetooth
15	GPIO8	I/O	Programmable input/output line
16	GPIO4	I/O	Programmable input/output line
17	NC		
18	GPIO9	I/O	Programmable input/output line
19	VDD_3V3	Vdd	Power supply voltage 3.3V
20	GND	Vss	Power Ground
21	GPIO10	I/O	Programmable input/output line
22	UART_RTS	I/O	UART request to send active low
23	UART_CTS	I	UART clear to send active low
24	UART_TX	O	UART data output
25	UART_RX	I	UART data input
26	SWCLK	I/O	Debugging through the clk line(Default)
27	SWDAT	I/O	Debugging through the data line(Default)
28	RESET	I	External reset input: Active LOW, with an inter an internal pull-up. Set this pin low reset to initial state.
29	GND	Vss	Power Ground

4. PHYSICAL INTERFACE

4.1 Power Supply

The transient response of the regulator is important. If the power rails of the module are supplied from an external voltage source, the transient response of any regulator used should be 20μs or less. It is essential that the power rail recovers quickly.

4.2 RF Interface

For this module, the default mode of the antenna is internal antenna.

The user can connect the 50 ohm antenna directly to the RF port.

- 2402–2480 MHz
- TX output power of +9dBm.
- Receiver to achieve maximum sensitivity -95dBm @ 0.1% BLE

4.3 Serial Interfaces

4.3.1 UART

FSC-BT982 provides one channels of Universal Asynchronous Receiver/Transmitters(UART)(Full-duplex asynchronous communications). The UART Controller performs a serial-to-parallel conversion on data received from the peripheral and a parallel-to-serial conversion on data transmitted from the CPU. Each UART Controller channel supports ten types of interrupts.

This is a standard UART interface for communicating with other serial devices. The UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

When the module is connected to another digital device, UART_RX and UART_TX transfer data between the two devices.

This module output is at 3.3V CMOS logic levels (tracks VCC). Level conversion must be added to interface with an RS-232 level compliant interface.

Table 3: Possible UART Settings

Parameter	Possible Values	
Baudrate	Minimum	1200 baud (≤2%Error)
	Standard	115200bps(≤1%Error)
	Maximum	921600bps(≤1%Error)
Flow control		Supports Automatic Flow Control (CTS and RTS lines)
Parity		None, Odd or Even
Number of stop bits		1 /1.5/2
Bits per channel		5/6/7/8

When connecting the module to a host, please make sure to follow .

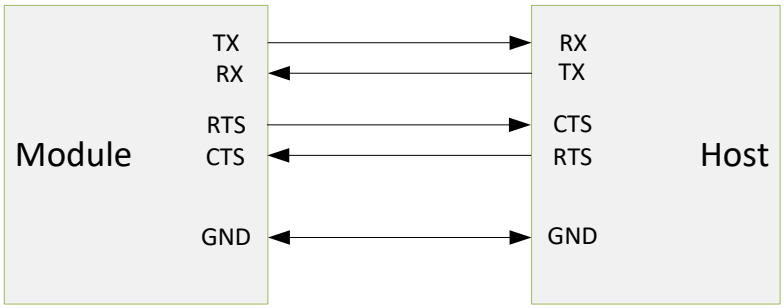


Figure 4: UART Connection

5. ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

Absolute maximum ratings for supply voltage and voltages on digital and analogue pins of the module are listed below. Exceeding these values causes permanent damage.

The average PIO pin output current is defined as the average current value flowing through any one of the corresponding pins for a 100mS period. The total average PIO pin output current is defined as the average current value flowing through all of the corresponding pins for a 100mS period. The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

Table 4: Absolute Maximum Rating

Parameter	Min	Max	Unit
VDD_3V3 DC Power Supply	-0.3	+3.6	V
T_{ST} - Storage Temperature	-20	+85	°C

5.2 Recommended Operating Conditions

Table 5: Recommended Operating Conditions

Parameter	Min	Type	Max	Unit
VDD_3V3 DC Power Supply	3.2	3.3	3.4	V
T_A - Operating Temperature	-10	25	+85	°C

5.3 RF characteristics

Table 6: Transmitter Characteristics

Parameter	Min	Type	Max	Unit
Operating Frequency	2400		2480	MHz
RF output power	-20	0	9	dBm
Out of band emission 2 MHz (GFSK)		-40		dBm
Out of band emission 3 MHz(GFSK)		-48		dBm
20dB bandwidth		0.9		MHz

Table 7: BLE Receiver Characteristics

Parameter	Min	Type	Max	Unit
High Gain mode, Sensitivity @0.1%		-95		dBm
Standard Gain mode, Sensitivity @0.1%		-92		dBm
Maximum Input Power		0		dBm
Co-channel C/I, Basic Rate, GFSK		7		dB
ACS C/I 1MHz, Basic Rate, GFSK		5.5	7	dB
ACS C/I 2MHz, Basic Rate, GFSK		-36	-34	dB
ACS C/I 3MHz, Basic Rate, GFSK		-43		dB
ACS C/I Image channel, Basic Rate, GFSK		-34		dB
C/I 1 MHz adjacent to image channel, Basic Rate, GFSK		-28		dB

Table 8: BT Receiver Characteristics

Parameter	Min	Type	Max	Unit
Basic Rate, GFSK, BER<0.1%, Dirty Tx on		-92		dBm
EDR, π /4 DQPSK, BER<0.01%, Dirty Tx on		-93		dBm
EDR, 8PSK, BER<0.01%, Dirty Tx on		-83		dBm
Maximum Input Power		0		dBm
Co-channel C/I, EDR, π /4 DQPSK		10.5		dB
ACS C/I 1MHz, EDR, π /4 DQPSK		-8		dB
ACS C/I 2MHz, EDR, π /4 DQPSK				dB
ACS C/I 3MHz, EDR, π /4 DQPSK		-54		dB
ACS C/I Image channel, EDR, π /4 DQPSK		-27		dB
C/I 1 MHz adjacent to image channel, EDR, π /4 DQPSK		-43		dB
Co-channel C/I, EDR, 8PSK		20		dB
ACS C/I 1MHz, EDR, 8PSK		0		dB
ACS C/I 2MHz, EDR, 8PSK		-20		dB
ACS C/I 3MHz, EDR, 8PSK		-45		dB
ACS C/I Image channel, EDR, 8PSK		-18		dB
C/I 1 MHz adjacent to image channel, EDR, 8PSK		-33		dB

6. MSL & ESD

Table 9: MSL and ESD

Parameter	Value
MSL grade:	MSL 3
ESD grade:	Human Body Model: Class-2 Machine Model: Class-B

7. RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages

contain desiccate (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the below **next table** and follow instructions specified by IPC/JEDEC J-STD-033.

Note: The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the below **next table**, the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccate and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60%RH.

Table 10: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Feasycom surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

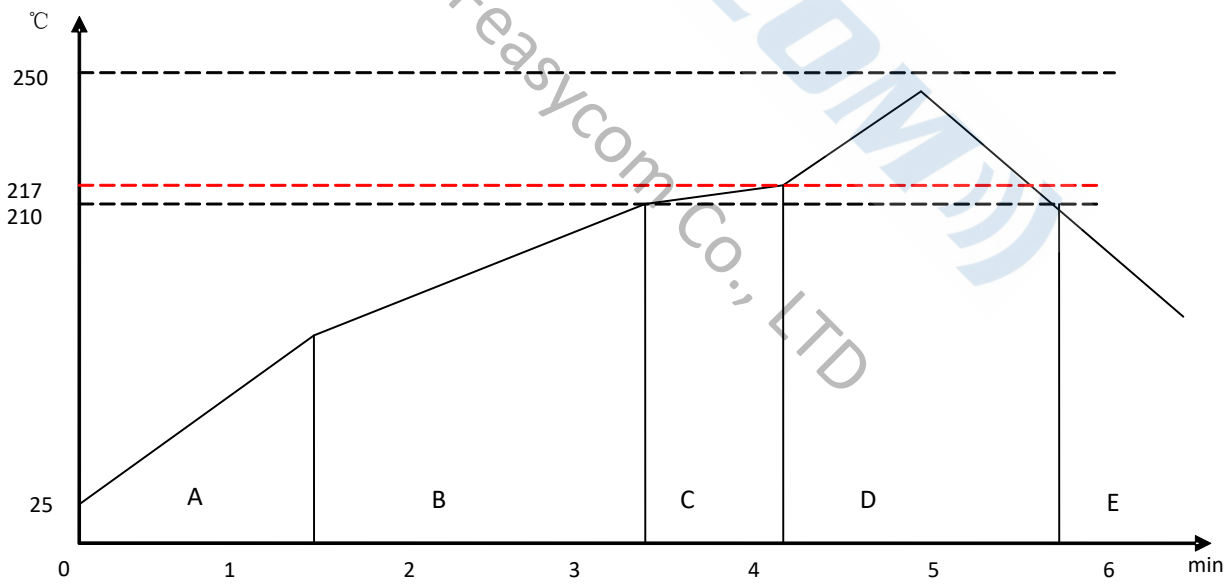


Figure 5: Typical Lead-free Re-flow

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

Equilibrium Zone 2 (C) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

8. MECHANICAL DETAILS

8.1 Mechanical Details

FSC-BT982 Dimension: 16.55mm(L)x10.88mm(W)x2.2mm(H)

Tolerance:+/-0.25mm

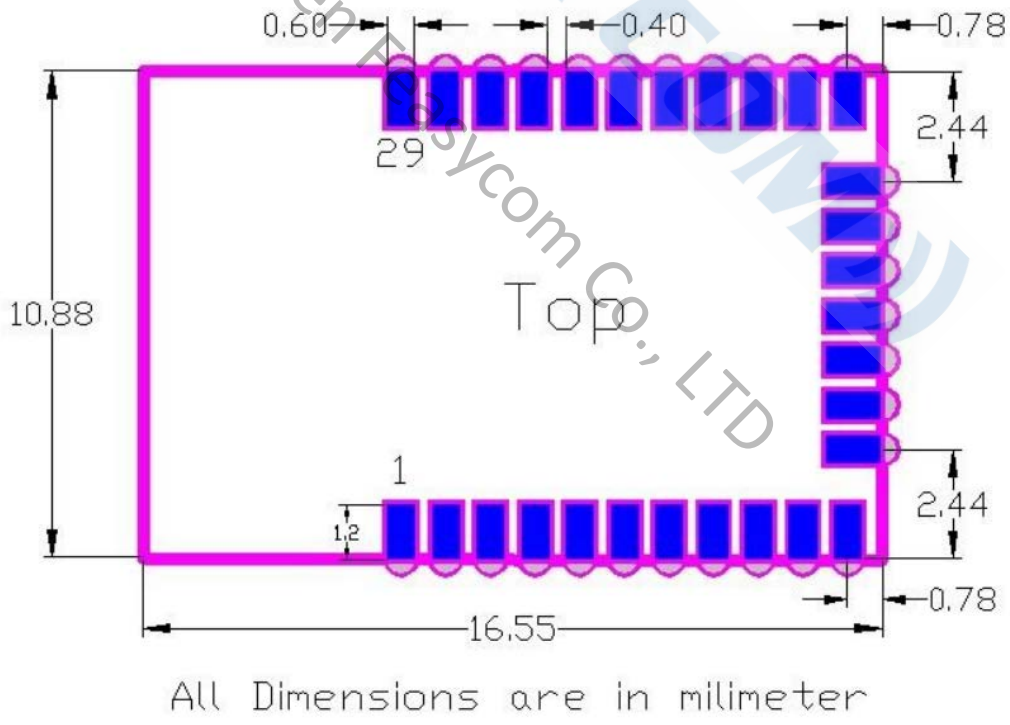


Figure 6: FSC-BT982 footprint

9. HARDWARE INTEGRATION SUGGESTIONS

9.1 Soldering Recommendations

FSC-BT982 is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

9.2 Layout Guidelines(Internal Antenna)

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.

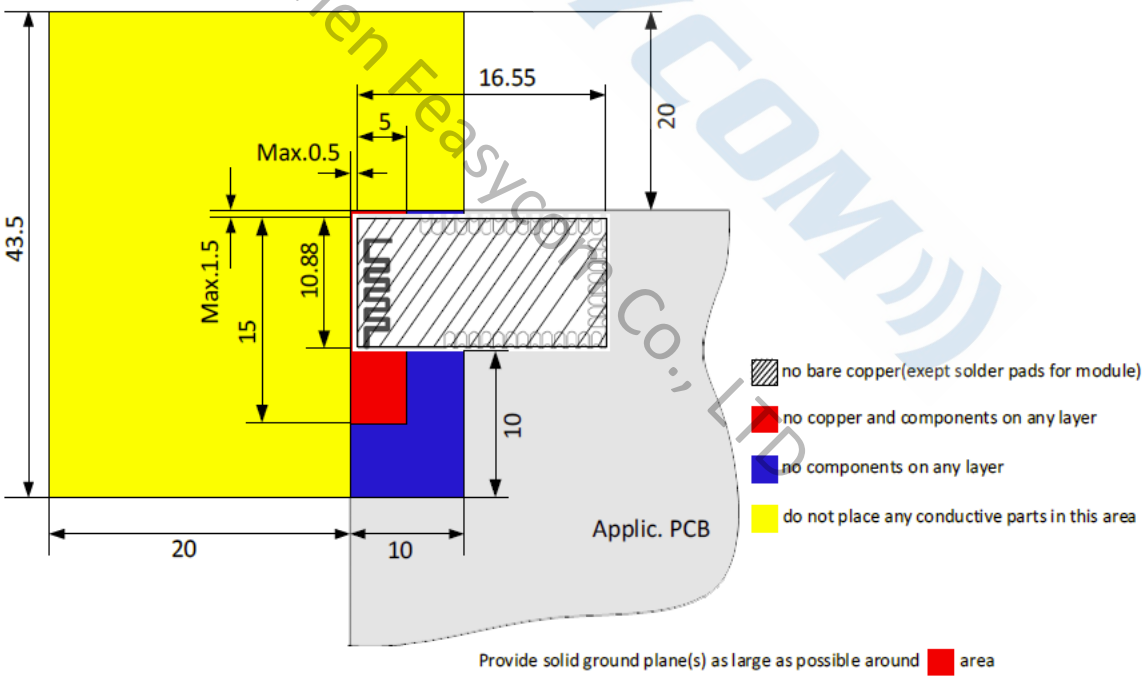


Figure 7: FSC-BT982 Restricted Area

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the

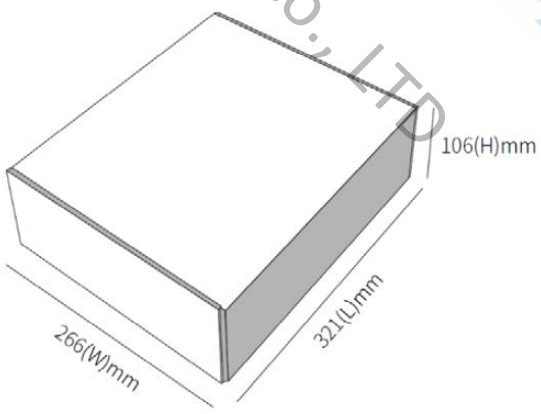
line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

10. PRODUCT PACKAGING INFORMATION

10.1 Default Packing

Figure 12: Tray vacuum

10.2 Packing box(Optional)



* If require any other packing, must be confirmed with customer

* Package: 1000PCS Per Carton (Min Carton Package)

Figure 13: Packing Box

11. APPLICATION SCHEMATIC