FSC-BW101

Bluetooth 5.0 + Dual-band 1x1 802.11ac Module Datasheet

Version 1.7

Revision History

Version	Data	Notes	Approved By
1.0	2018/05/04	Initial Version	Devin Wan
1.1	2018/09/03	1, Update BT 4.1 to BT 4.2. 2, Update module thickness, external antenna interface, block diagram and application circuit diagram	Devin Wan
1.2	2019/04/16	1, PCB changed from 4-layer board to 6-layer board, optimize circuit design 2, Correction module and package image 3, The Notice about the stencil making	Devin Wan
1.3	2019/04/28	Add solder mask slivers next to the locating hole of the shield to prevent soldering tin from diffusing to the bonding pad on the back of the module.	Devin Wan
1.4	2019/06/06	Update BT 4.2 to BT 5.0.	Devin Wan
1.5	2020/06/17	Add the comparison description of FSC-BW101 & FSC-BW101B and update the application circuit diagram.	Devin Wan
1.6	2020/10/23	Selection of version	Devin Wan
1.7	2023/01/03	Revised the Storage Temperature range into -40°C ~ +85°C, modified wrong descriptions in sections 5.5 and 9.2	Devin Wan

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Contents

1. INTRODUCTION

Overview

FSC-BW101 uses the gauge level IC QCA1023，it is a highly integrated Wi-Fi / Bluetooth combo module to support 1X1 SISO. FSC-BW101 single-Module provides the highest level of integration for Industry. It is connectivity systems with integrated two spatial streams IEEE802.11a/b/g/n/ac MAC/baseband/radio, Bluetooth 5.0 + HS enabling seamless integration of WLAN/BT and Low Energy technology.

FSC-BW101 implements highly sophisticated enhanced collaborative coexistence hardware mechanisms and algorithms, which ensure that WLAN and Bluetooth collaboration is optimized for maximum performance. As a result, enhanced overall quality for simultaneous voice, video, and transmission is achieved.

FSC-BW101 is an appropriate product for designers who want to add wireless capability to their products. Let all of the system high design flexibility, short development cycle, and quick time-to-market.

General Features

- IEEE 802.11a/b/g/n/ac radio with virtual-simultaneous dual-band operation
- Provides a highly integrated WLAN system-on-chip (SOC)for 5 GHz 802.11ac, or 2.4GHz/5GHz 802.11n WLAN applications
- Supports BT5.0 + HS, BLE and ANT+ and backward compatibility with BT 1.x and BT2.x + Enhanced Data Rate
- Supports a single-ended RF port for cleaner and lower cost design
- Supports 20MHz/40MHz at 2.4GHz and supports 20MHz, 40MHz, or 80MHz at 5GHz
- Supports BT_WLAN coexistence and ISM-LTE coexistence
- Operates on one 3.3-volt power supply and an I/O supply of 1.8V or 3.3V. Both WLAN and BT power management use advanced power-saving techniques such as:
  - Gating clocks to idle or inactive blocks
  - Voltage scaling to specific blocks in certain states
  - Fast start and settling circuits reduce TX
  - Active duty cycles
  - Processor frequency scaling
  - Other techniques to optimize power consumption across all operating states

  --Includes additional features such as:
    - Low –density parity check(LDPC)
    - 1.5Kb of Module one-time programmable (OTP) memory to eliminate the need for an external flash and to further reduce the external component count and BOM cost

  --Supports BT for class 1 and class 2 power-level transmissions without requiring an external PA
- Module WLAN driver execution capable of supporting IEEE 802.11 functionality
- WLAN host interface options
- Low power SDIO3.0/SDIO2.0 interface for WLAN and UART/PCM interface for BT
- BT host digital interface(which can be used concurrently with the below interface)
- UART(Max Baud Rate 3.2Mbps)
- Single ended RF port for cleaner and low cost design
- 20/40MHz at 2.4GHz and 20/40/80MHz at 5GHz
- PCM for BT audio
- Stamp module suitable for Surface Mounted

Technology (SMT)

- Iron Shielding case
- Stamp-56 package
- Dimension(Iron Shielding Case) : 17mm(L) x 17mm(W) x 2.4mm(H)
- Operating Voltage : VDD_3V3_WL : 3.14 to 3.46V ; VDD_IO: 1.71 to 3.46V
- RoHS / REACH Compliant
- Industry Level

Bluetooth Features

- Bluetooth V5.0, and is backwards compatible with BT 1.X, 2.X + EDR, BT 3.X. and BT4.0
- BT for class 1 and class 2 power-level transmissions without requiring an external PA
- UART(Max Baud Rate 3.2Mbps)
- PCM for BT audio

WLAN Features

- IEEE 802.11ac compliant. (Support WPA, WPA2/WPA3)
- Single-stream spatial multiplexing up to 433.3 Mbps data rate.
- Supports 20, 40, and 80 MHz channels with optional SGI (256 QAM modulation).
- Full IEEE 802.11a/b/g/n legacy compatibility with enhanced performance.
- Low power SDIO3.0/SDIO2.0 interface for WLAN

Application

- Internet-of-Things (IoT) Applications, including:
  – Home and Building Automation
  – Low-Power Video Cameras
  – Thermostats
  – Access Control and Electronic Locks (E-Locks)
  – Asset Tracking and Real Time Location System (RTLS)

Tags
  – Cloud Connectivity
  – Internet Gateway
  – Appliances
  – Security Systems
  – Smart Energy
  – Industrial Control
  – Smart Plug and Metering
  – Wireless Audio
  – IP Network Sensor Nodes
  – Medical Devices

- Car audio and video system

Module picture as below showing

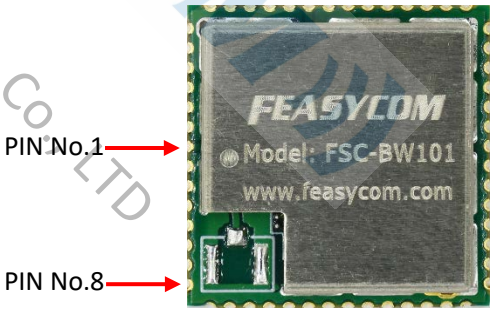


Figure 1: FSC-BW101 Picture

1.1 Selection of version

Order Number	Descriptions	Module picture as below showing
FSC-BW101 **(Default)**	PIN No.1 RF_IO_WIFI/BT PIN No.45 NC External antenna(stamp hole，PIN No.1)	
FSC-BW101B **(Optional)**	PIN No.1 NC PIN No.45 RF_IO_WIFI/BT External antenna(stamp hole，PIN No.45)	
FSC-BW101C **(Optional)**	PIN No.1 NC PIN No.45 NC External antenna (IPEX connector)	

- *See chapter 3.2 for details*

2. General Specification

Table 1: General Specifications

Categories	Features	Implementation
Bluetooth		
Bluetooth Standard		Bluetooth V5.0+EDR
Frequency Band		2402MHz~2480MHz
Interface		UART/PCM
WIFI		
Frequency Band		2412MHz~2484MHz /4900MHZ~5925MHz
Interface		SDIO
General		
Size		17mm × 17 mm × 2.4mm
Operating temperature		-40°C ~+85°C
Storage temperature		-40°C ~+85°C
VDD_3V3_WL		3.3V (Typ.)
VDD_IO		1.8V~3.3V (Typ.)
Miscellaneous	Lead Free	Lead-free and RoHS compliant
	Warranty	One Year
Humidity		10% ~ 90% non-condensing
MSL grade:		MSL 3
ESD grade:		Human Body Model: Pass ±2000 V, all pins Charge device model: Pass ±400 V, all pins

3. HARDWARE SPECIFICATION

3.1 Block Diagram and PIN Diagram

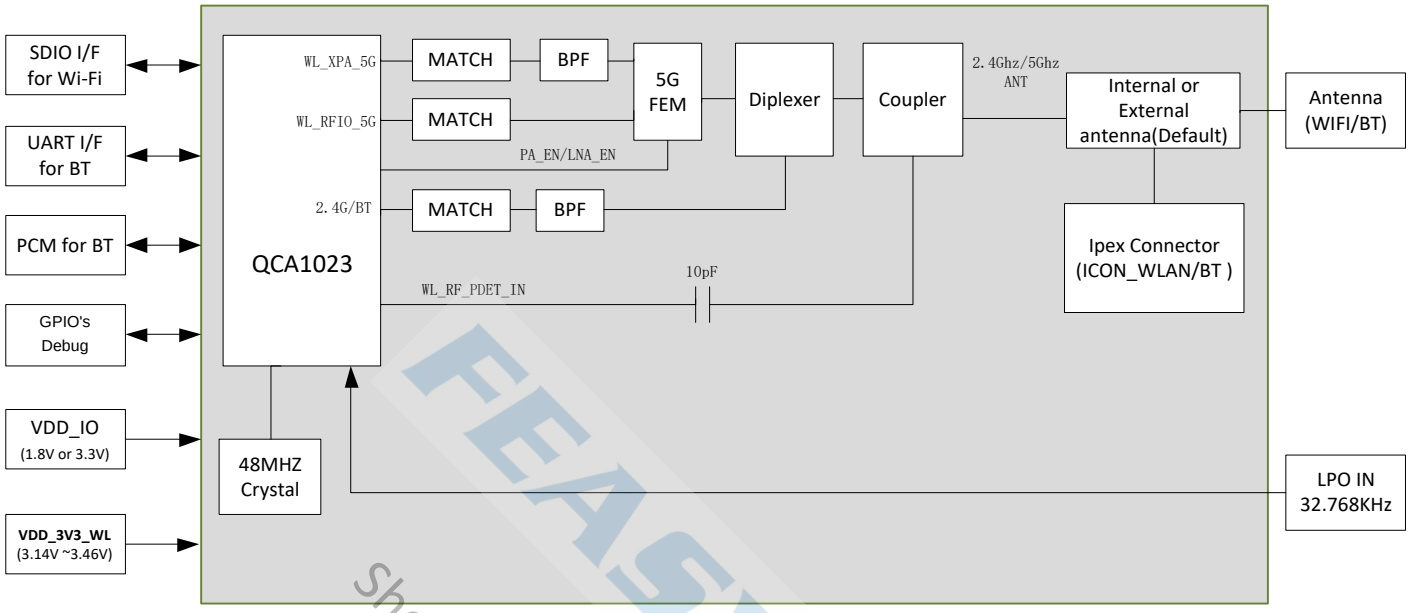


Figure 2: Block Diagram

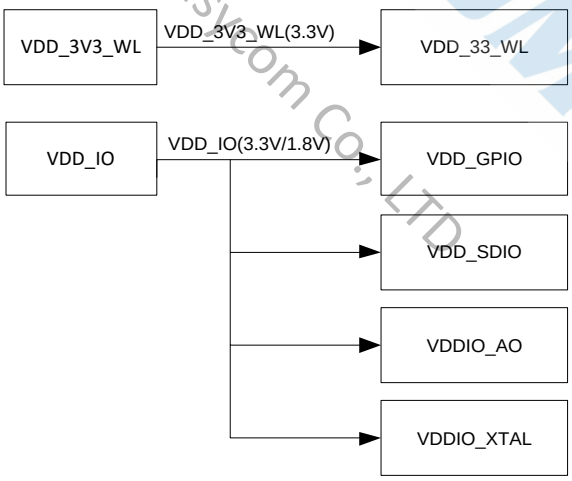


Figure 3: Block diagram of the power section

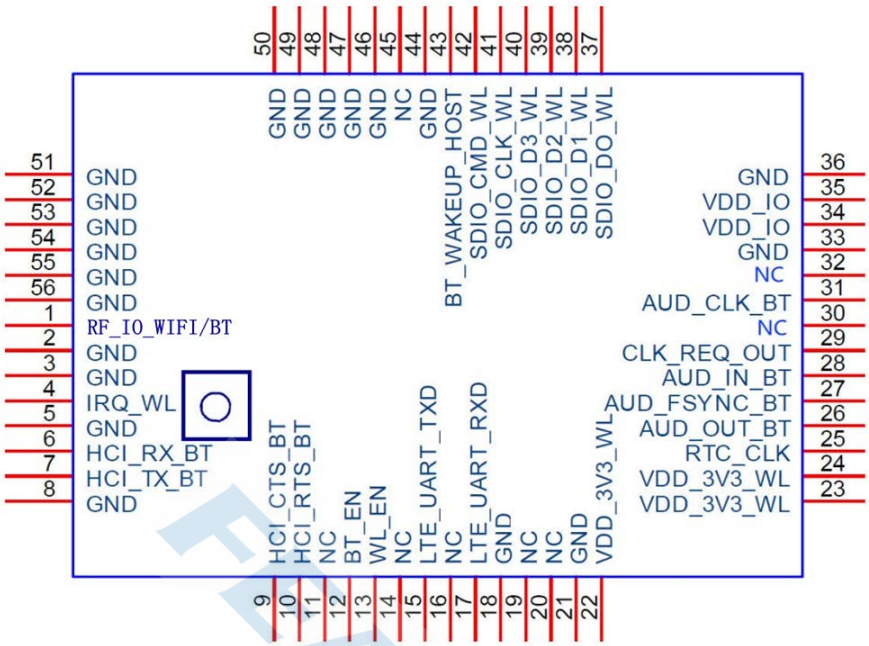


Figure 4: FSC-BW101 PIN Diagram(Top View)

3.2 PIN Definition Descriptions

Table 2: Pin definition

Pin	Pin Name	Type	Pin Descriptions	Notes
1	RF_IO_WIFI/BT	RF	WIFI 2.4G/5G RF and BT RF in/out port (FSC-BW101 only) ***** No function (FSC-BW101B and FSC-BW101C only，)***	
2	GND		Ground	
3	GND		Ground	
4	IRQ_WL	O	Wi-Fi Interrupt Request	
5	GND		Ground	
6	HCI_RX_BT	I	BT UART Data Input	
7	HCI_TX_BT	O	BT UART Data Output	
8	GND		Ground	
9	HCI_CTS_BT	I	BT UART I/F	
10	HCI_RTS_BT	O	BT UART I/F	
11	NC			
12	BT_EN	I	Bluetooth Function Enable(High Active)(BT_Reset)	
13	WL_EN	I	Wi-Fi Function Enable(High Active) (Wi-Fi_Reset)	
14	NC			
15	LTE_UART_TXD	O	LTE co-existence signal. LTE_UART_TXD	
16	NC			
17	LTE_UART_RXD	I	LTE co-existence signal. LTE_UART_RXD	
18	GND		Ground	
19	NC			
20	NC			

21	GND		Ground
22	VDD_WL_3V3	PWR	3.3V Supply Voltage
23	VDD_WL_3V3	PWR	3.3V Supply Voltage
24	VDD_WL_3V3	PWR	3.3V Supply Voltage
25	RTC_CLK	I	Sleep Clock(32.768kHz)
26	AUD_OUT_BT	O	BT PCM/I2S Bus. Data out ; NC if not used
27	AUD_FSYNC_BT	I	BT PCM/I2S Bus. Frame sync ; NC if not used.
28	AUD_IN_BT	I	BT PCM/I2S Bus. Data in ; NC if not used.
29	CLK_REQ_OUT	O	CLK_REQ Positive Polarity; Leave NC if not used.
30	NC		
31	AUD_CLK_BT	I	BT PCM/I2S Clock; NC if not used.
32	NC		
33	GND		Ground
34	VDD_IO	PWR	1.8V~3.3V Supply Voltage
35	VDD_IO	PWR	1.8V~3.3V Supply Voltage
36	GND		Ground
37	SDIO_D0_WL	I/O	SDIO Data Line 0
38	SDIO_D1_WL	I/O	SDIO Data Line1
39	SDIO_D2_WL	I/O	SDIO Data Line 2
40	SDIO_D3_WL	I/O	SDIO Data Line 3
41	SDIO_CLK_WL	I	WLAN SDIO Clock. Must be driven by the host
42	SDIO_CMD_WL	I	SDIO Command Input
43	BT_WALEUP_HOST	O	Host wakeup Bluetooth; NC if not used.
44	GND		Ground
45	NC		No function (FSC-BW101 and FSC-BW101C only) ***** WIFI 2.4G/5G RF and BT RF in/out port (FSC-BW101B only)***
46	GND		Ground
47	GND		Ground
48	GND		Ground
49	GND		Ground
50	GND		Ground
51	GND		Ground
52	GND		Ground
53	GND		Ground
54	GND		Ground
55	GND		Ground
56	GND		Ground

4. PHYSICAL INTERFACE

4.1 UART Interface

The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 3.2 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth 5.0 UART HCI specification: H4, a custom Extended H4, and H5. The default baud rate is 115.2 Kbps.

The UART supports the 3-wire H5 UART transport, as described in the Bluetooth specification (Three-wire UART Transport Layer). Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals.

FSC-BW101 UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers.

FSC-BW101 UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

Table 3: Possible UART Settings

Parameter	Possible Values	
Baudrate	Minimum	9600 baud (≤0%Error)
	Standard	115200bps(≤1.6%Error)
	Maximum	3.2Mbps(≤0%Error)
Flow control		Supports Automatic Flow Control (CTS and RTS lines)
Parity		None, Odd or Even
Number of stop bits		1
Bits per channel		8

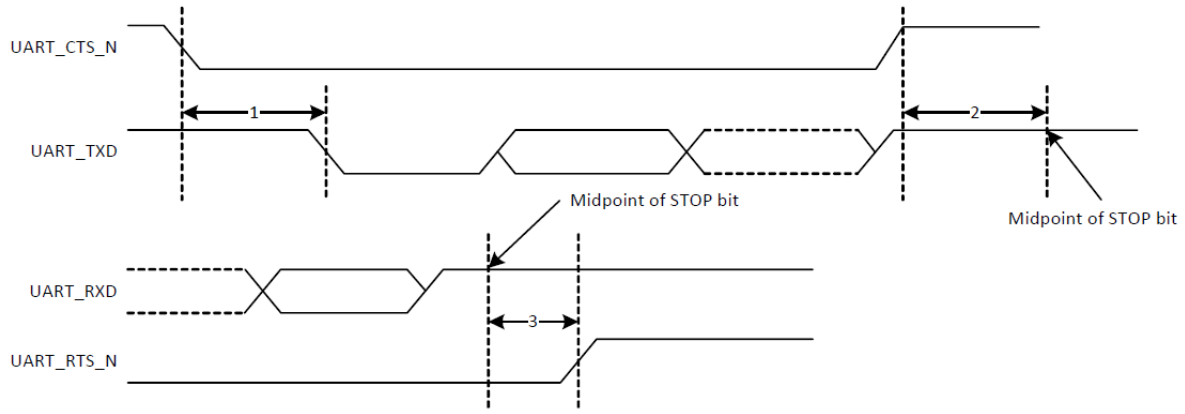


Figure 5: UART Timing

Table 4: UART Timing Specifications

Parameter	Min	Type	Max	Unit
Delay time, UART_CTS_N low to UART_TXD valid			1.5	Bit period
Setup time, UART_CTS_N high before midpoint of stop bit			0.5	Bit period
Delay time, midpoint of stop bit to UART_RTS_N high			0.5	Bit period

4.2 Bluetooth PCM Interface

The pulse coded modulation (PCM) interface connects the FSC-BW101 to the phone's audio interface, or to peripheral devices, such as a codec. The PCM interface circuits use digital I/O pins that receive power from the VDD_IO supply. Their I/O performance specifications meet the requirements stated.

FSC-BW101 PCM interface has been designed to minimize audio latency. The typical audio latencies for various packet types as follows.

Table 5: Typical PCM interface audio latency

Packet type	Audio latency
HV3/EV3 Tesco=6,Wesco=0	4.4mS
EV3 Tesco=6,Wesco=2	5.7mS
EV3 Tesco=6,Wesco=4	6.9mS

The PCM interface is configured to operate as master or slave. In each case, the PCM_IN pin is the data receive terminal (an input), and the PCM_OUT pin is the data transmit terminal (an output). The clock and sync pins function as inputs or outputs, depending on whether FSC-BW101 PCM interface is configured as master or slave:

- When FSC-BW101 PCM interface is the master : PCM_CLK and PCM_SYNC are outputs from the device to the PCM bus slave(s).
- When FSC-BW101 PCM interface is the slave : PCM_CLK and PCM_SYNC are inputs to the device from the PCM bus master.

Table 6: PCM interface specifications

Parameter	Min	Type	Max	Unit
Clock rate(Slave)—Determined by the master	64	-	2048	KHz
Clock rate(Master)—(32MHz *N/4000),in which N is an integer	64	-	2048	KHz
Frame size	1	8	256	Bits
Slot size	1	13	16	Bits
Slot number—Number of slots that can be configured per frame	1	-	32	Slots/frame

Example timing diagrams and specifications for slave and master configurations are described in the following tables and illustrations.

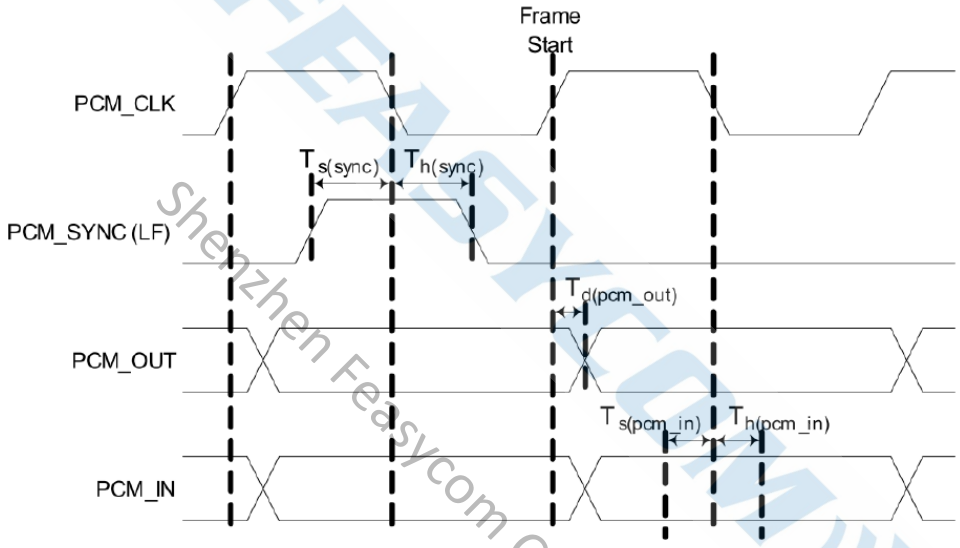


Figure 6: PCM interface timing diagram(slave)

Table 7: PCM interface timing in slave mode

Parameter	Min	Type	Max	Unit
PCM bit clock frequency	64	-	2048	KHz
Setup time PCM_SYNC to PCM_CLK fall	0	-	-	ns
Hold time PCM_CLK fall to PCM_SYNC fall	150	-	-	ns
Delay from PCM_CLK rise to PCM_OUT	0	-	150	ns
Setup time PCM_IN to PCM_CLK fall	0	-	-	ns
Hold time PCM_IN after PCM_CLK fall	150	-	-	ns

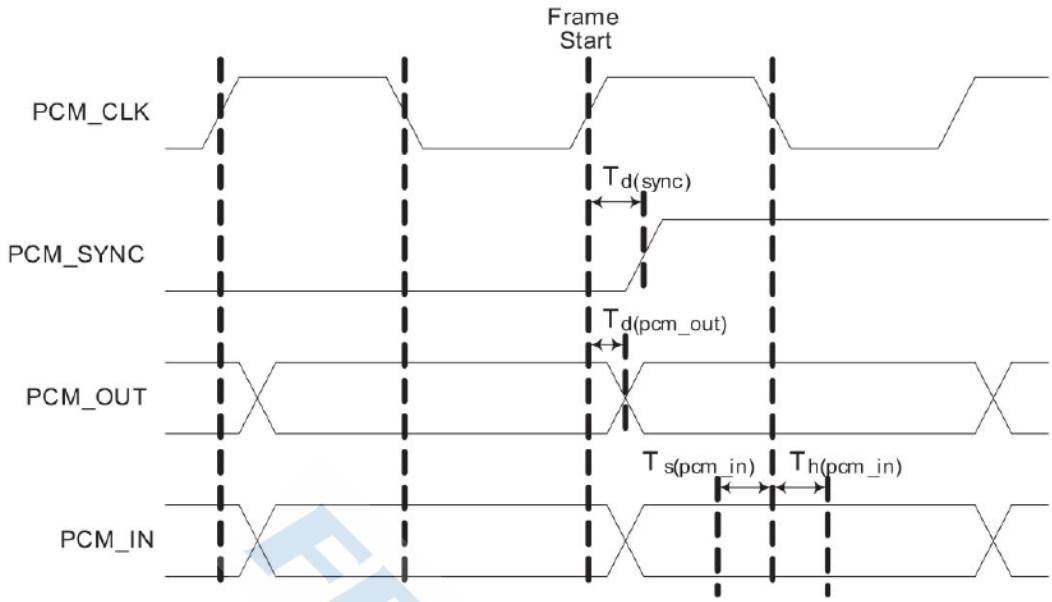


Figure 7: PCM interface timing diagram(master)

Table 8: PCM interface timing in master mode

Parameter	Min	Type	Max	Unit
PCM bit clock frequency	64	-	2048	KHz
Delay from PCM_CLK rise to long SYNC	-10	-	50	ns
Delay from PCM_CLK rise to PCM_OUT	-10	-	50	ns
Setup time PCM_IN to PCM_CLK fall	50	-	-	ns
Hold time PCM_IN after PCM_CLK fall	150	-	-	ns

4.3 WLAN Host Interfaces

4.3.1 SDIO V3.0

The module WLAN section supports SDIO version 3.0, including the new UHS-I modes:

- DS: Default speed (DS) up to 25 MHz, including 1- and 4-bit modes (3.3V signaling).
- HS: High speed up to 50 MHz (3.3V signaling).
- SDR12: SDR up to 25 MHz (1.8V signaling).
- SDR25: SDR up to 50 MHz (1.8V signaling).
- SDR50: SDR up to 100 MHz (1.8V signaling).
- SDR104: SDR up to 208 MHz (1.8V signaling).
- DDR50: DDR up to 50 MHz (1.8V signaling).

Note: The QCA1023 is backward compatible with SDIO v2.0 host interfaces.

The SDIO interface also has the ability to map the interrupt signal on to a GPIO pin for applications requiring an interrupt different from the one provided by the SDIO interface. The ability to force control of the gated clocks from within the device is also provided.

SDIO mode is enabled by strapping options. Refer to next Table WLAN GPIO Functions and Strapping Options.

The following three functions are supported:

- Function 0 Standard SDIO function (Max. BlockSize/ByteCount = 32B)
- Function 1 Backplane Function to access the internal system-on-chip (SoC) address space (Max. BlockSize/ByteCount = 64B)
- Function 2 WLAN Function for efficient

Table 9: SDIO Pin Description

SD 4-Bit Mode	
DATA0	Data line 0
DATA1	Data line 1 or Interrupt
DATA2	Data line 2 or Read Wait
DATA3	Data line 3
CLK	Clock
CMD	Command line

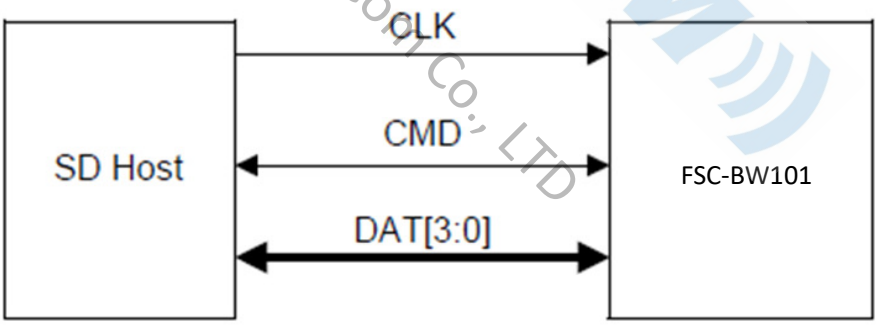


Figure 8: Signal Connections to SDIO Host (SD 4-Bit Mode)

4.3.2 SDIO Default Mode Timing

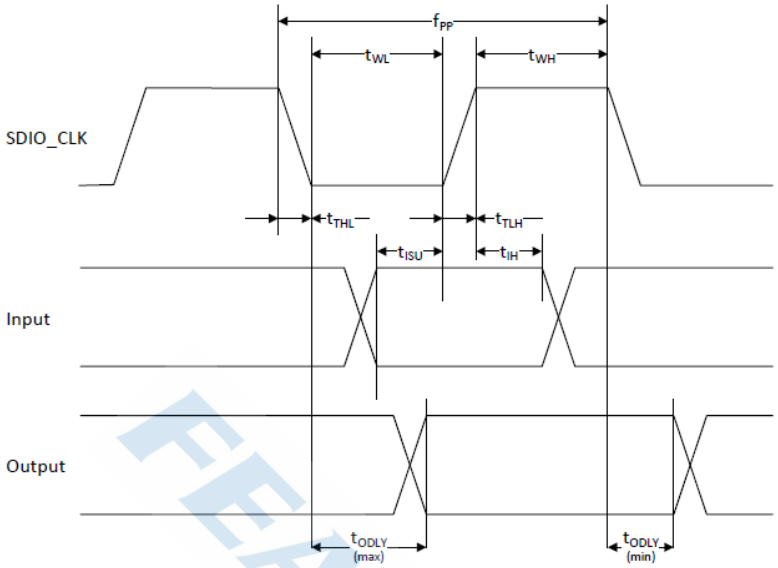


Figure 9: SDIO Bus Timing (Default Mode)

Table 10: SDIO Bus Timing[a] Parameters (Default Mode)

Parameter	Min	Type	Max	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL[b])				
Frequency – Data Transfer mode	0	-	25	MHz
Frequency – Identification mode	0	-	400	KHz
Clock low time	10	-	-	ns
Clock high time	10	-	-	ns
Clock rise time	8	-	10	ns
Clock fall time	0	-	10	ns
Inputs: CMD, DAT (referenced to CLK)				
Input setup time	5	-	-	ns
Input hold time	5	-	-	ns
Outputs: CMD, DAT (referenced to CLK)				
Output delay time – Data Transfer mode	0	-	14	ns
Output delay time – Identification mode	0	-	50	ns

a. Timing is based on CL <= 40pF load on CMD and Data.

b. Min. (Vih) = 0.7 X VDDIO and max (Vil) = 0.2 X VDDIO.

4.3.3 SDIO High-Speed Mode Timing

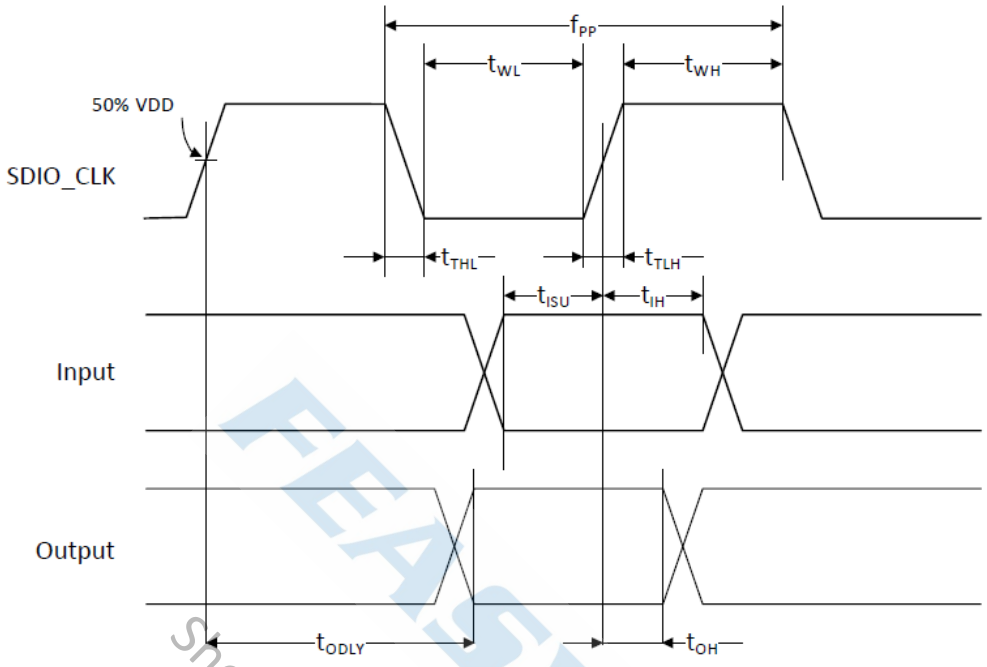


Figure 10: SDIO Bus Timing (Default Mode)

Table 11: SDIO Bus Timing[a] Parameters (High-Speed Mode)

Parameter	Min	Type	Max	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL[b])				
Frequency – Data Transfer mode	0	-	50	MHz
Frequency – Identification mode	0	-	400	KHz
Clock low time	7	-	-	ns
Clock high time	7	-	-	ns
Clock rise time	-	-	3	ns
Clock fall time	-	-	3	ns
Inputs: CMD, DAT (referenced to CLK)				
Input setup time	6	-	-	ns
Input hold time	2	-	-	ns
Outputs: CMD, DAT (referenced to CLK)				
Output delay time – Data Transfer mode	-	-	14	ns
Output hold time	2.5	-	-	ns
Total system capacitance (each line)	-	-	40	

a. Timing is based on CL <= 40pF load on CMD and Data.

b. Min. (Vih) = 0.7 X VDDIO and max (Vil) = 0.2 X VDDIO.

4.3.4 SDIO Bus Timing Specifications in SDR Modes

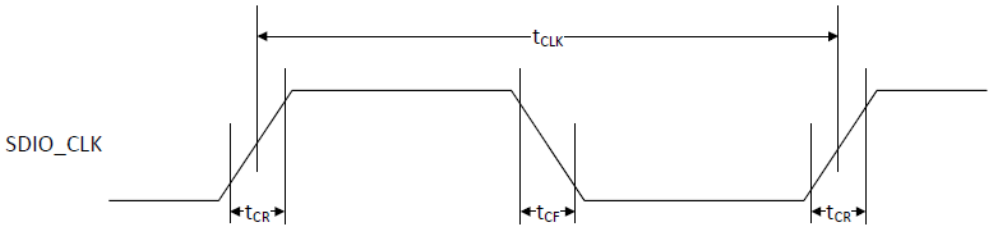


Figure 11: SDIO Clock Timing (SDR Modes)

Table 12: SDIO Bus Clock Timing Parameters (SDR Modes)

Parameter	Min	Type	Max	Unit	Unit
	40	-	-	ns	SDR12 mode
	20	-	-	ns	SDR25 mode
	10	-	-	ns	SDR50 mode
	4.8	-	-	ns	SDR104 mode
	-	-	3	ns	tCR, tCF < 2.00 ns (max.) @100 MHz, CCARD = 10 pF tCR, tCF < 0.96 ns (max.) @208 MHz, CCARD = 10 pF
Clock duty cycle	30	-	70	%	ns

4.3.5 Device Input Timing

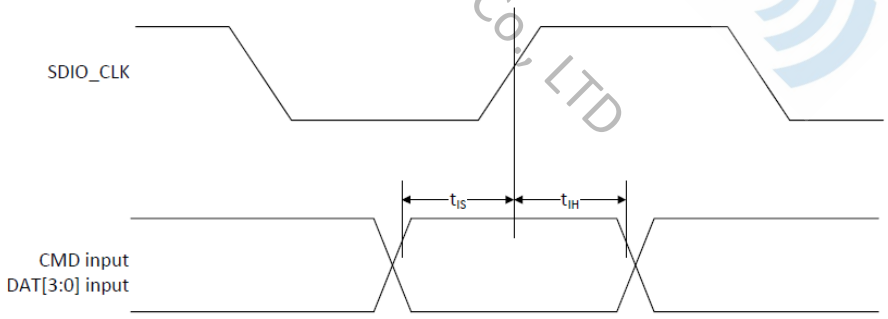


Figure 12: SDIO Bus Input Timing (SDR Modes)

Table 13: SDIO Bus Input Timing Parameters (SDR Modes)

Symbol	Min	Type	Max	Unit	Unit
SDR104 Mode					
t_{IS}	1.4	-	-	ns	C_{CARD} = 10 pF, VCT = 0.975V
t_{IH}	0.8	-	-	ns	C_{CARD} = 5 pF, VCT = 0.975V
SDR50 Mode					
t_{IS}	3.0	-	-	ns	C_{CARD} = 10 pF, VCT = 0.975V
t_{IH}	0.8	-	-	ns	C_{CARD} = 5 pF, VCT = 0.975V

SDR25 Mode					
t_{IS}	3.0	-	-	ns	C_{CARD} = 10 pF, VCT = 0.975V
t_{IH}	0.8	-	-	ns	C_{CARD} = 5 pF, VCT = 0.975V
SDR12 Mode					
t_{IS}	3.0	-	-	ns	C_{CARD} = 10 pF, VCT = 0.975V
t_{IH}	0.8	-	-	ns	C_{CARD} = 5 pF, VCT = 0.975V

4.3.6 Device Output Timing

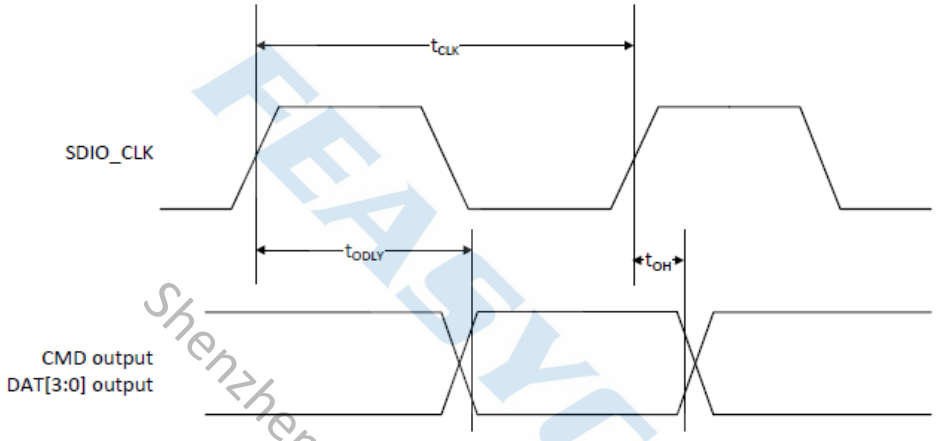


Figure 13: SDIO Bus Output Timing (SDR Modes up to 100MHz)

Table 14: SDIO Bus Output Timing Parameters (SDR Modes up to 100 MHz)

Symbol	Min	Type	Max	Unit	Unit
t_{ODLY}	–	-	7.5	ns	t_{CLK} ⩾10 ns C_L= 30 pF using driver type B for SDR50
t_{ODLY}	–	-	14.0	ns	t_{CLK} ⩾20 ns C_L= 40 pF using for SDR12, SDR25
T_{OH}	1.5	-	-	ns	Hold time at the t_{ODLY} (min) C_L= 15 pF

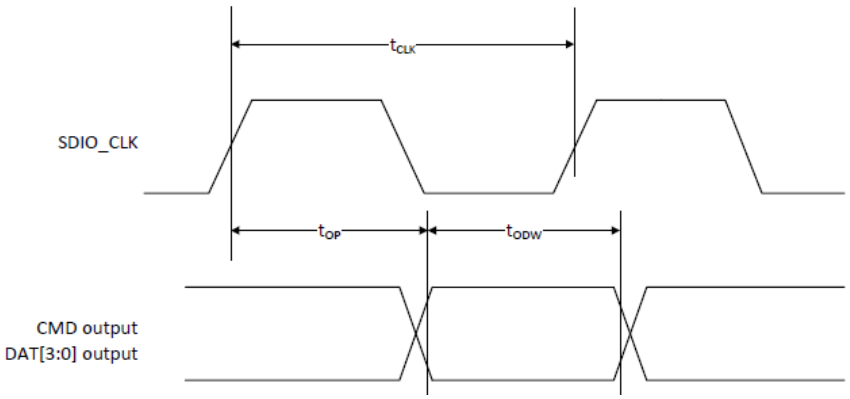


Figure 14: SDIO Bus Output Timing (SDR Modes 100 MHz to 208 MHz)

Table 15: SDIO Bus Output Timing Parameters (SDR Modes 100 MHz to 208 MHz)

symbol	Min	Type	Max	Unit	Unit
t_{OP}	0	-	2	UI	Card output phase
Δt_{OP}	-350	-	+1550	ps	Delay variation due to temp change after tuning
t_{ODW}	0.60	-	-	UI	t_{ODW}=2.88 ns @208 MHz

- Δt_{OP} = +1550 ps for junction temperature of Δt_{OP} = 90 degrees during operation
- Δt_{OP} = − 350 ps for junction temperature of Δt_{OP} = − 20 degrees during operation
- Δt_{OP} = +2600 ps for junction temperature of Δt_{OP} = − 20 to +125 degrees during operation

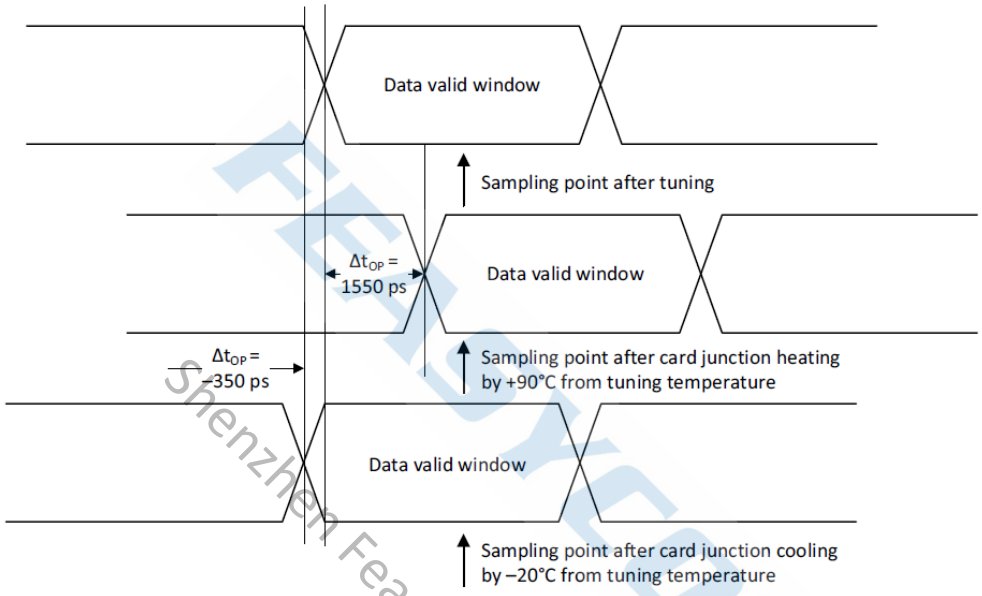


Figure 15: ΔtOP Consideration for Variable Data Window (SDR 104 Mode)

4.3.7 SDIO Bus Timing Specifications in DDR50 Mode

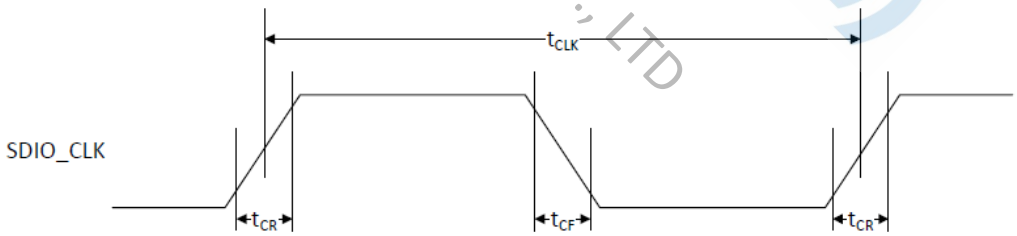


Figure 16: SDIO Clock Timing (DDR50 Mode)

Table 16: SDIO Bus Clock Timing Parameters (DDR50 Mode)

Parameter	Min	Type	Max	Unit	Unit
	20	-	7.5	ns	DDR50 mode
	-	-	0.2 x t_{CLK}	ns	t_{CR}, t_{CF} < 4.00 ns (max) @50 MHz, C_{CARD} = 10 pF
Clock duty cycle	45	-	55	%	-

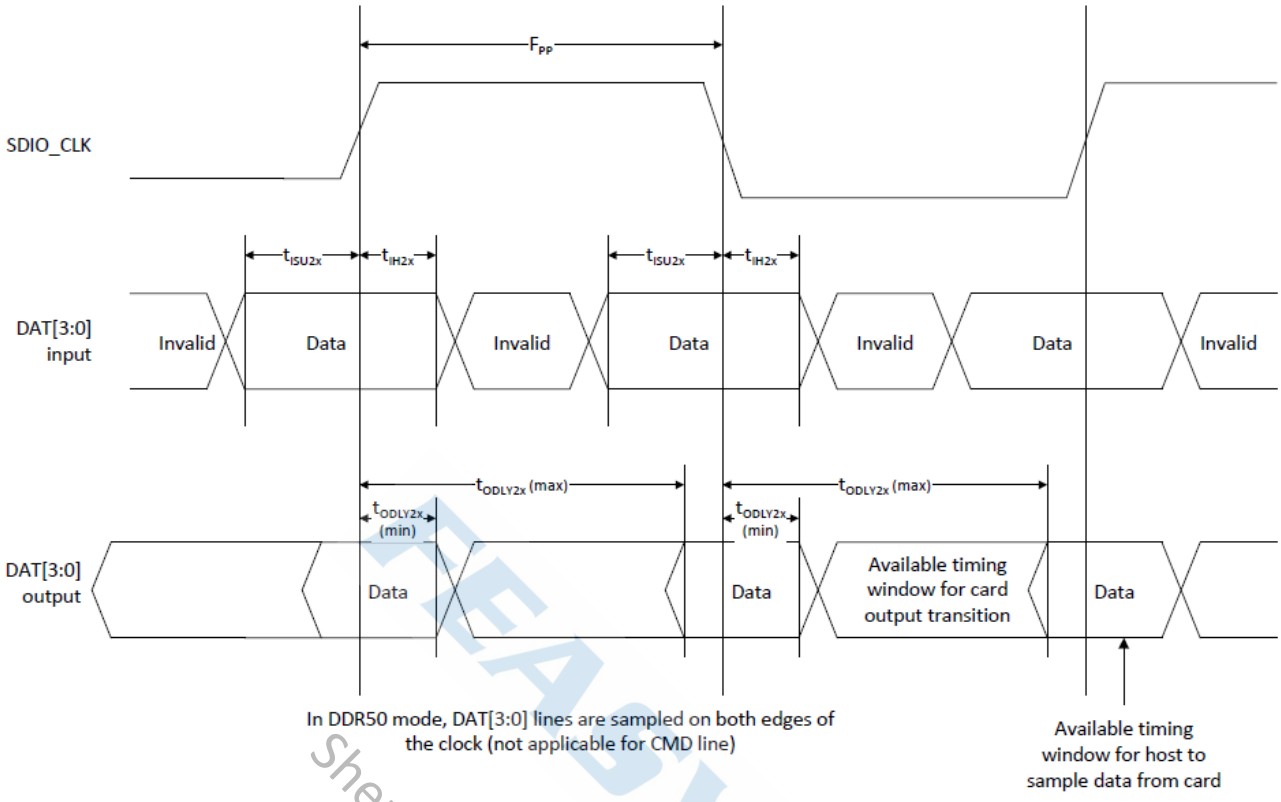


Figure 17: SDIO Data Timing (DDR50 Mode)

Table 17: SDIO Bus Timing Parameters (DDR50 Mode)

Parameter	Min	Type	Max	Unit	Comments
Input CMD					
Input setup time	6	-	-	ns	C_{CARD} < 10pF (1 Card)
Input hold time	0.8	-	-	ns	C_{CARD} < 10pF (1 Card)
Outputs CMD					
Output delay time	-	-	13.7	ns	C_{CARD} < 30pF (1 Card)
Output hold time	1.5	-	-	ns	C_{CARD} < 15pF (1 Card)
Input DAT					
Input setup time	3	-	-	ns	C_{CARD} < 10pF (1 Card)
Input hold time	0.8	-	-	ns	C_{CARD} < 10pF (1 Card)
Outputs DAT					
Output delay time	-	-	7.0	ns	C_{CARD} <25pF (1 Card)
Output hold time	1.5	-	-	ns	C_{CARD} < 15pF (1 Card)

5. ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

All measurements are referenced at the module pins unless otherwise indicated. All specifications are over process and voltage unless otherwise indicated.
Over operating free-air temperature range (unless otherwise noted)

Table 18: Absolute Maximum Rating

Parameter	Min	Max	Unit
VDD_3V3_WL(SWREG Supply Input)	-0.3	+3.6	V
VDD_IO(DC supply voltage for digital I/O)	-0.3	+3.6	V
Operating temperature (T_A)	-40	+85	°C
Storage temperature (T_{stg})	-40	+85	°C
Maximum junction temperature(T_j)		+125	°C

5.2 Recommended Operating Conditions

Table 19: Recommended Operating Conditions

Parameter	Min	Type	Max	Unit
VDD_3V3_WL	3.14	3.3	3.46	V
VDD_IO	1.71	1.8~3.3	3.46	°C
Operating temperature (T_A)	-40	25	+85	°C
Storage temperature (T_{stg})	-40	25	+85	°C
High-level input voltage	0.7 X VDD_IO		VDD_IO + 0.3	V
Low-level input voltage	-0.3		0.3 X VDD_IO	V
Input low leakage current	-5.0		5.0	uA
High-level output voltage	0.9 X VDD_IO		VDD_IO	V
Low-level output voltage	0		0.1 X VDD_IO	V
High-level output current	3			mA
Low-level output current			-11	mA

5.3 RF Characteristic

5.3.1 WLAN RF Characteristics(Transmitter)

Table 20: WLAN Transmitter

Characteristics	Condition	EVM	Min	Type	Max	Unit
2.4GHz						
Output Power	11M CCK		13	15	18	dBm
	6M OFDM		14	14	17	dBm
	54M OFDM	-25	11	13	16	dBm
	6.5M,MCS0(HT20)		12	13	17	dBm
	65M,MCS7(HT20)	-27	10	11	15	dBm
	6.5M,MCS0(HT40)		11	12	16	dBm
	65M,MCS7(HT40)	-27	10	11	15	dBm
	180M,MCS9(VHT40)	-32	8	9	13	dBm
5GHz						
Output Power	54M OFDM	-25	10	12	16	dBm
	65M,MCS7(HT20)	-27	8	12	16	dBm
	65M,MCS7(HT20)	-27	8	12	16	dBm
	78M,MCS8(VHT20)	-30	8	12	16	dBm
	180M,MCS9(VHT40)	-32	8	12	16	dBm
	390M,MCS9(VHT80)	-32	6	9	12	dBm

5.3.2 WLAN RF Characteristics(Receive)

Table 21: WLAN Receive

Characteristics	Condition	Min	Type	Max	Unit
2.4GHz					
Sensitivity	11M CCK	-89	-86	-76	dBm
	54M OFDM	-76	-74	-65	dBm
	65M,MCS7(HT20)	-74	-72	-64	dBm
5GHz					
Sensitivity	54M OFDM	-78	-76	-65	dBm
	65M,MCS7(HT20)	-76	-74	-64	dBm
	130M,MCS7(HT40)	-74	-72	-64	dBm
	78M,MCS8(VHT20)	-70	-68	-59	dBm
	180M,MCS9(VHT40)	-67	-65	-54	dBm
	390M,MCS9(VHT80)	-65	-62	-51	dBm

5.3.3 Bluetooth RF Characteristics

Table 22: Bluetooth RF Characteristics

Characteristics	Condition	Min	Type	Max	Unit
BT Transmitter, GFSK					
RF output power		9	11		dBm
Power control step		2	4	8	dB
BT Receiver Characteristics, Basic rate receiver					
Sensitivity	GFSK, BER = 0.1%		-88		dBm
	Pi/4-DQPSK, BER = 0.01%		-90		dBm
	8DPSK, BER = 0.01%		-82		
Max. useable input power	GFSK, BER = 0.1%	-5			dBm
	Pi/4-DQPSK, BER = 0.1%	-10			dBm
	8DPSK, BER = 0.1%	-10			dBm
BLE RF Characteristics					
BLE Transmitter output power			2		dBm
BT Receiver Characteristics, Low energy receiver	BER <= 0.1%		-92		dBm

5.4 Digital pad internal pull resistor

Table 23: Digital pad internal pull resistor

Internal Pull Resistor	VDD_IO = 1.8V		VDD_IO = 3.3V	
	R(KΩ)		R(KΩ)	
	Min	MAX	Min	MAX
Pull down	23	72	24	60
Pull up	70	168	49	95

5.5 Power Up/Down Sequence

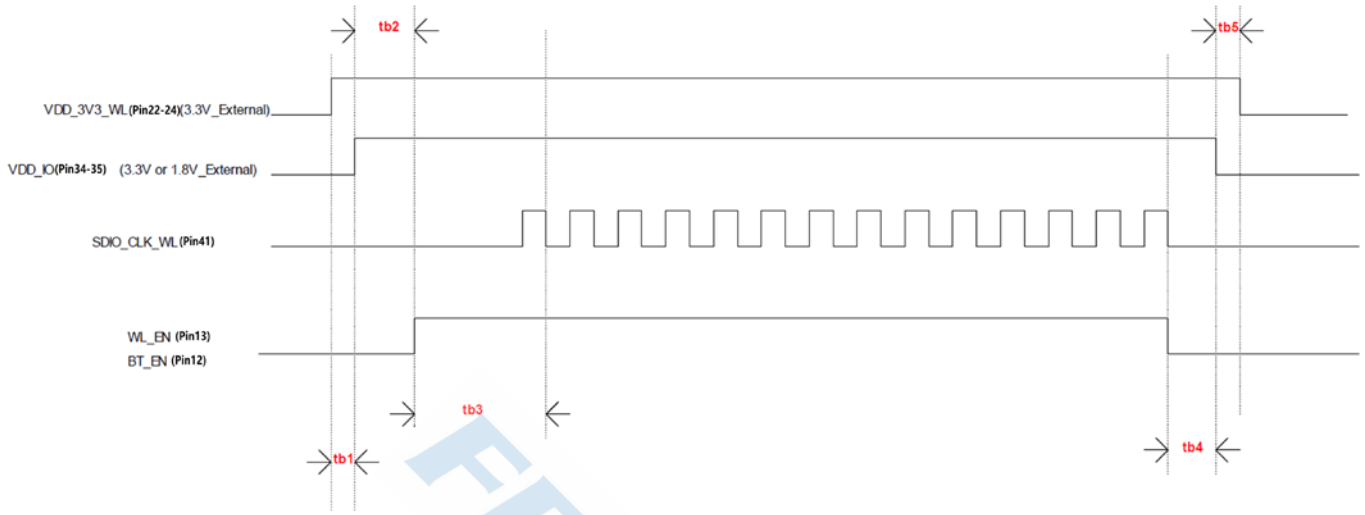


Figure 18: Power on and power off timing Sequence

Table 24: Power on and power off timing Sequence

Parameter	Min	Type	Max	Unit
tb1--VDD_3V3_WL to VDD_IO input active	2			uS
tb2--VDD_IO to WL_EN/BT_EN input active	10			uS
tb3--WL_EN/BT_EN valid to SDIO enable by Host	1			mS
tb4--WL_EN/BT_EN de-assert to VDD_IO ramping down	10			uS
tb5--WL_EN/BT_EN de-assert to VDD_3V3_WL ramping down	2			uS

5.6 Power Consumption

Table 25: Power Consumption:

Internal Pull Resistor	Voltage	Power Consumption(mA)(Max)
VDD_3V3_WL	3.3V	500
VDD_IO	3.3V	300
Testing Condition:	2.4GHz Tx MCS0 6.5Mbps	

FSC-BW101 Module Power Consumption:

500mA @ VDD_3V3_WL(Maximum) and 300mA @ VDD_IO(Maximum)

Suggest customer design power capacity are 1000mA@VDD_3V3_WL and 500mA @ VDD_IO for FSC-BW101 Module.

6. MSL & ESD

Table 26: MSL and ESD

Parameter	Value
MSL grade:	MSL 3
ESD grade	**Electrostatic discharge**
ESD – Human-body model (HBM) rating, JESD22-A114-F (Total samples from one wafer lot)	Pass ±2000 V, all pins
ESD – Charge-device model (CDM) rating, JESD22-C101-D (Total samples from one wafer lot)	Pass ±400 V, all pins

7. RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccate (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the below and follow instructions specified by IPC/JEDEC J-STD-033.

Note: The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the below , the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccate and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60%RH.

Notice (注意) :

Feasycom module must use Step-Stencil, suggestion using the stencil thickness about 0.16-0.2mm,

it could be modify with the product.

使用我司模块，须使用阶梯钢网，建议阶梯钢网厚度0.16-0.20mm，可根据自己产品适应性，进行相应调整.

Table 27: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Feasycom surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

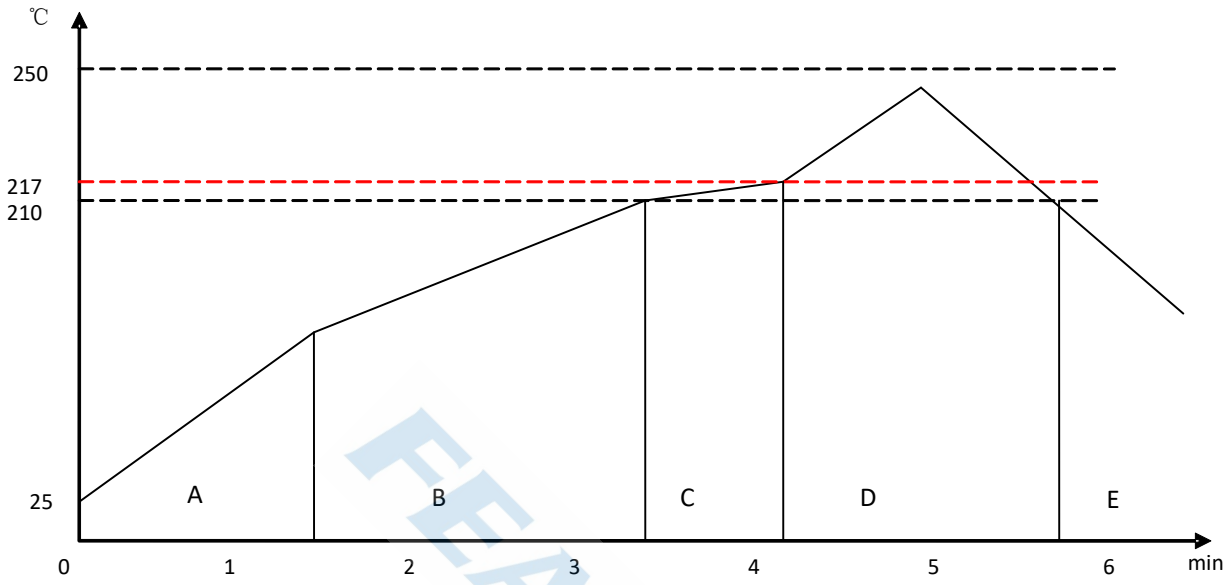


Figure 19: Typical Lead-free Re-flow

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

Equilibrium Zone 2 (C) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

8. MECHANICAL DETAILS

8.1 Mechanical Details

- Dimension: 17mm(W) x 17mm(L) x 2.4mm(H) Tolerance: ±0.1mm
- Module size: 17mm X 17mm Tolerance: ±0.2mm
- Pad size: 1.5mmX0.75mm Tolerance: ±0.1mm
- Pad pitch: 1.1mm Tolerance: ±0.1mm
- The tolerance of residual board edge after board separated: less than 0.5mm
  (分板后边角残留板边误差：不大于0.5mm)

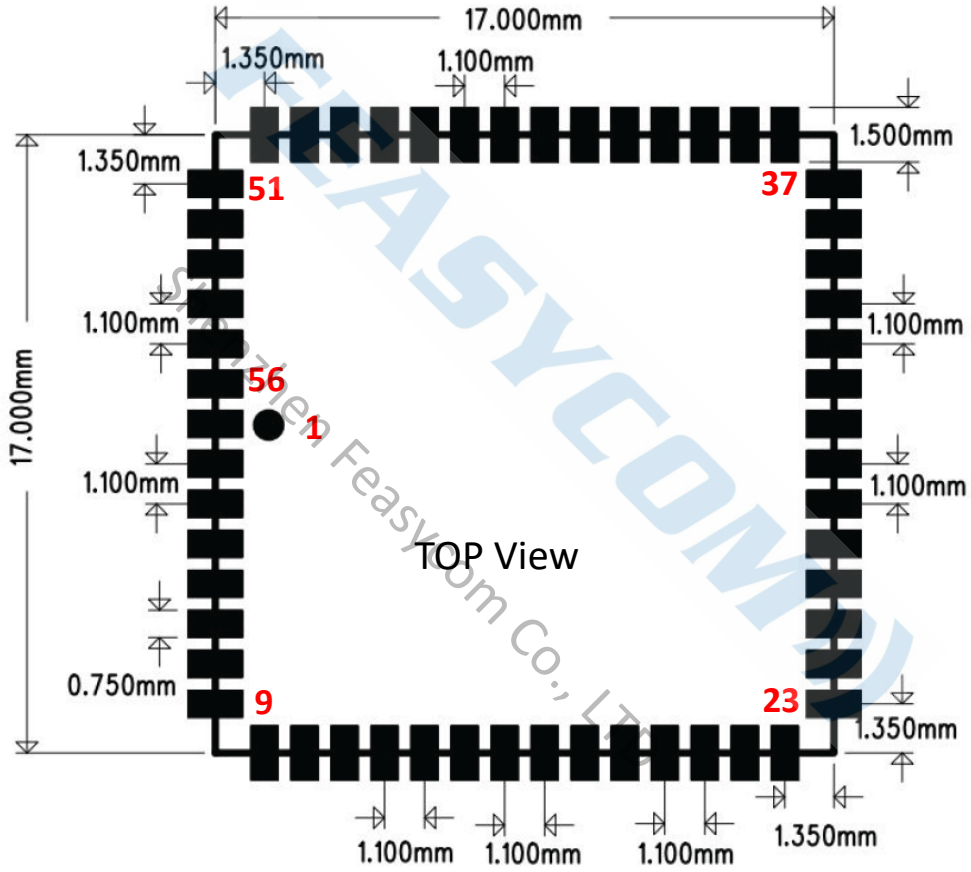


Figure 20: FSC-BW101 footprint Layout Guide (Top View)

9. HARDWARE INTEGRATION SUGGESTIONS

9.1 Soldering Recommendations

FSC-BW101 is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

9.2 Layout Guidelines(Internal Antenna)

Important Note: The antenna of FSC-BW101 needs to support both 2.4GHz and 5.8GHz dual frequency bands. We recommend using external FPC dual-band antennas instead of PCB onboard antennas. The following are general ins tructions for PCB onboard antennas for reference only.

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.

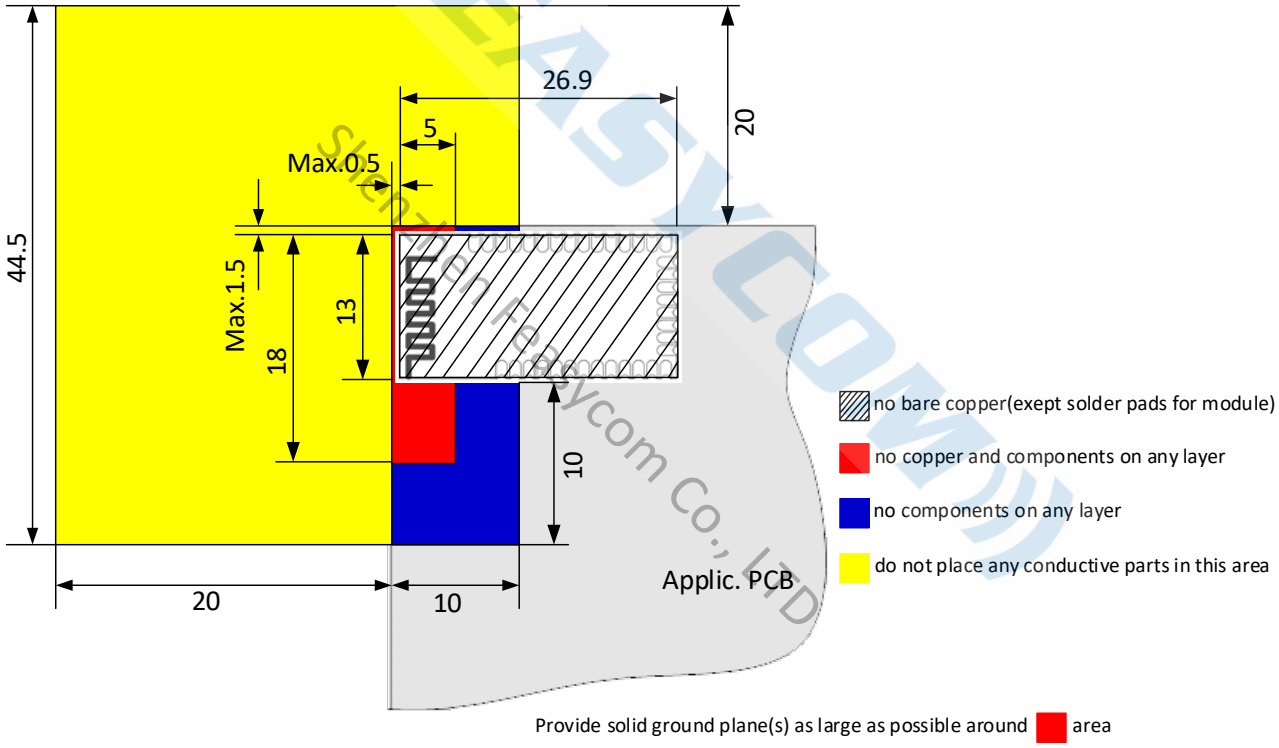


Figure 21: Restricted Area (Design schematic, for reference only. Unit: mm)

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

9.3 Layout Guidelines(External Antenna)

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

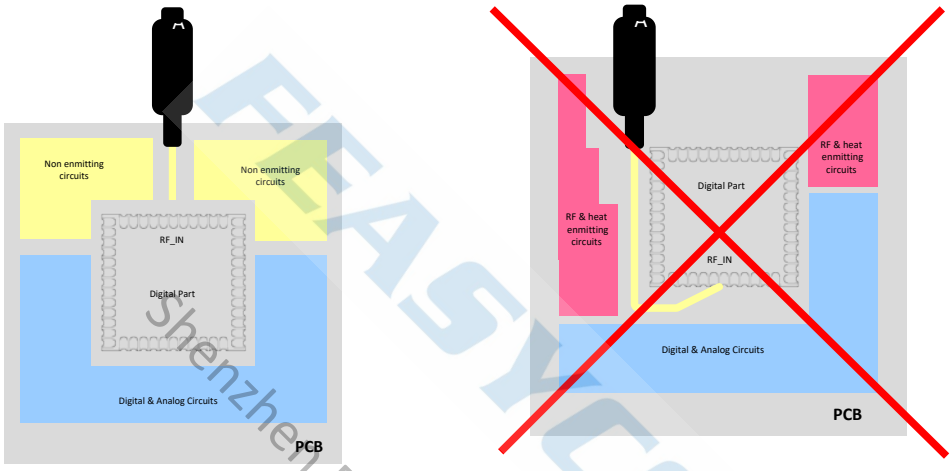


Figure 22: Placement the Module on a System Board

9.3.1 Antenna Connection and Grounding Plane Design

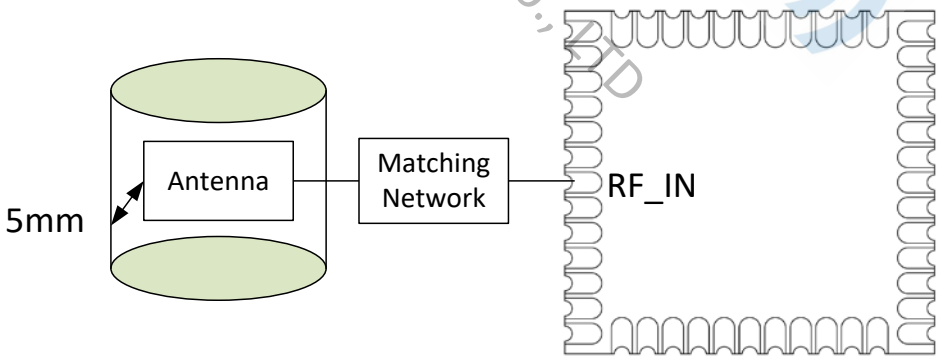


Figure 23: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.

- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

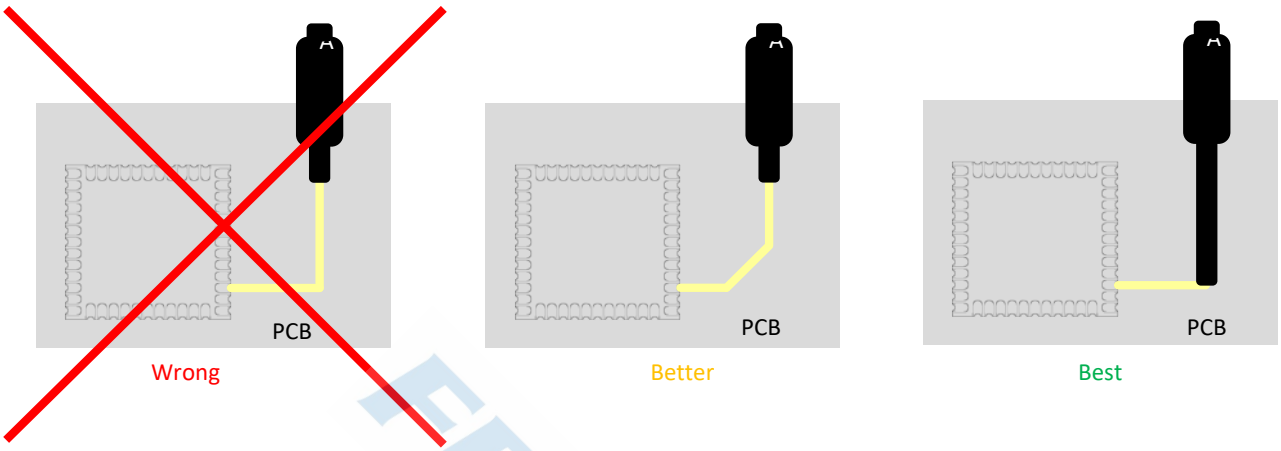


Figure 24: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

9.4 SDIO Lines Layout Guideline

The following SDIO line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive 8mA.

SDIO_CMD_WL

SDIO_CLK_WL

SDIO_D0_WL ~ SDIO_D3_WL

The route length of these signals be less than 15 cm and the line impedance be less than 50Ω

9.5 HCI Lines Layout Guideline

The following HCI line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive 4 ~ 8mA

HCI_RX_BT

HCI_TX_BT

HCI_CTS_BT

HCI_RTS_BT

The route length of these signals be less than 15 cm and the line impedance be less than 50Ω

9.6 PCM Lines Layout Guideline

The following HCI line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive 4 mA

AUD_FSYNC_BT(PCM_SYNC)

AUD_CLK_BT(PCM_CLK)

AUD_OUT_BT(PCM_OUT)

AUD _IN_BT(PCM_IN)

The route length of these signals be less than 15 cm and the line impedance be less than 50Ω

9.7 RTC Clock(32.768kHz) Lines Layout Guideline

Follow the same guidelines recommended for the fast clock, It is extremely important that the RTC_CLK trace not be routed next to any digital signals and near the analog audio signals. Furthermore, no digital signals should be routed above or below the RTC_CLK trace to avoid coupling.

9.8 Power Trace Lines Layout Guideline

VDD_3V3_WL Trace Width: 40mil

VDD_IO Trace Width: 20mil

9.9 Ground Lines Layout Guideline

A Complete Ground in Ground Layer.

Add Ground Through Holes to FSC-BW101 Module Ground Pads

Decoupling Capacitors close to FSC-BW101 Module Power and Ground Pads

10. PRODUCT PACKAGING INFORMATION

10.1 Default Packing

a, Tray vacuum

b, Tray Dimension: 140mm * 265mm

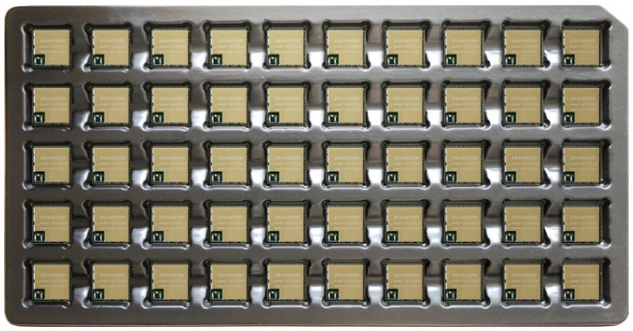
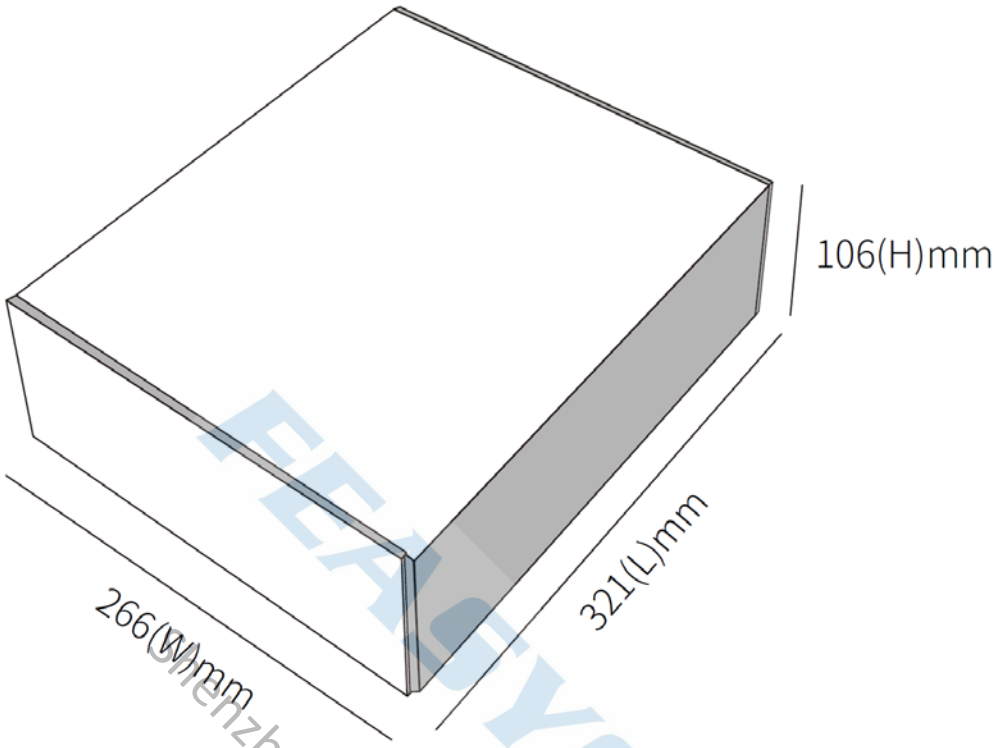


Figure 25: Tray vacuum

10.2 Packing box(Optional)



* If other packing is required, please confirm with the customer

* Packing: 1000pcs per carton (Minimum packing quantity)

* **The outer packing size is for reference only, please refer to the actual size**

Figure 26: Packing Box

11. APPLICATION SCHEMATIC