FSC-BT1038x

DATASHEET V1.1

1 INTRODUCTION

Overview

FSC-BT1038x it is a Bluetooth dual-mode module series. It supports LE Audio and classic Bluetooth.

FSC-BT1038x integrates an ultra-low-power DSP and application processor with embedded flash memory, a high-performance stereo codec, a power management subsystem, I^2S, LED drivers and ADC I/O.

Both cores use external flash to execute code, making it easy for user to differentiate products from new features without delaying the development

By default, FSC-BT1038x module is equipped with powerful and easy-to-use Feasycom firmware. It's easy to use and completely encapsulated. Feasycom firmware enables users to access Bluetooth functionality with simple ASCII commands delivered to the module over serial interface - it's just like a Bluetooth modem.

Therefore, FSC-BT1038x provides an ideal solution for developers who want to integrate Bluetooth wireless technology into their design.

Features

- Snapdragon Sound for lossless music streamin
- Qualified to Bluetooth® v5.4 specification
- 240 MHz Qualcomm® Kalimba™ audio DSP
- High-performance 24-bit audio interface
- cVc™ : 1-mic Qualcomm® cVc™ speaker noise reduction and echo cancellation technology (FSC-BT1038A)
  1 or 2 mic Qualcomm® headset speech processing (FSC-BT1038B)
- Digital interfaces: I^2S/PCM/SPDIF
- Active Noise Cancellation: Hybrid, Feedforward, and Feedback modes, using Digital or Analog Mics, enabled using license keys available from Qualcomm® (FSC-BT1038B)
- Supports aptX, aptX HD, aptX Lossless, aptX Adaptive(enabled using license key)
- Amazon Voice Services, Google Assistant
- Both analog-to-digital converter (ADC)s and the digital-to-analog converter (DAC) support sample rates of 8 kHz, 16 kHz, 32 kHz, 44.1 kHz, 48 kHz, 96 kHz. The DAC also supports 192 kHz and 384 kHz.
- Serial interfaces: UART, Bit Serializer (I^2C/SPI), USB 2.0
- Qualcomm® Bluetooth High Speed Link
- Bluetooth, Bluetooth Low Energy, and mixed topologies supported
- Class 1 support
- Power Consumption: Music Streaming (A2DP): ~5 mA

Application

- Wireless speakers/headphones

2 General Specification

Table 2-1：General Specifications

Categories	Features	Implementation
Bluetooth		
	Chip	FSC-BT1038A（QCC3083） FSC-BT1038B（QCC3084）
	Bluetooth Standard	Bluetooth v5.4
	Frequency Band	2402MHz~2480MHz
	Transmit Power	Basic Rate :+10 dBm (Typ VBAT=3.7V)
	Receiver	Basic rate: -96dBm (Typ VBAT=3.7V)
	Interface	UART/I²S/PCM/USB
Size		13mm × 26.9 mm × 2.2mm
Operating temperature		-40°C ~+85°C,
Storage temperature		-40°C ~+85°C
Supply Voltage		3.0V~4.2V
VDD_IO		1.8V~3.3V
Miscellaneous	Lead Free Warranty	Lead-free and RoHS compliant One Year
Humidity		10% ~ 90% non-condensing
MSL grade:		MSL 3
ESD grade:		Human Body Model: Pass ±2000 V Charge device model: Pass ±500 V

3 HARDWARE SPECIFICATION

3.1 Block Diagram and PIN Diagram

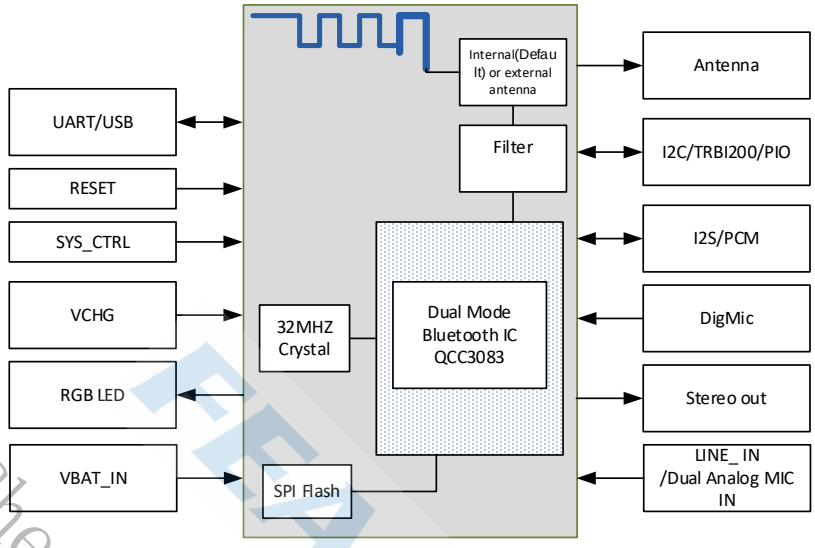

Figure 3-1:Block Diagram

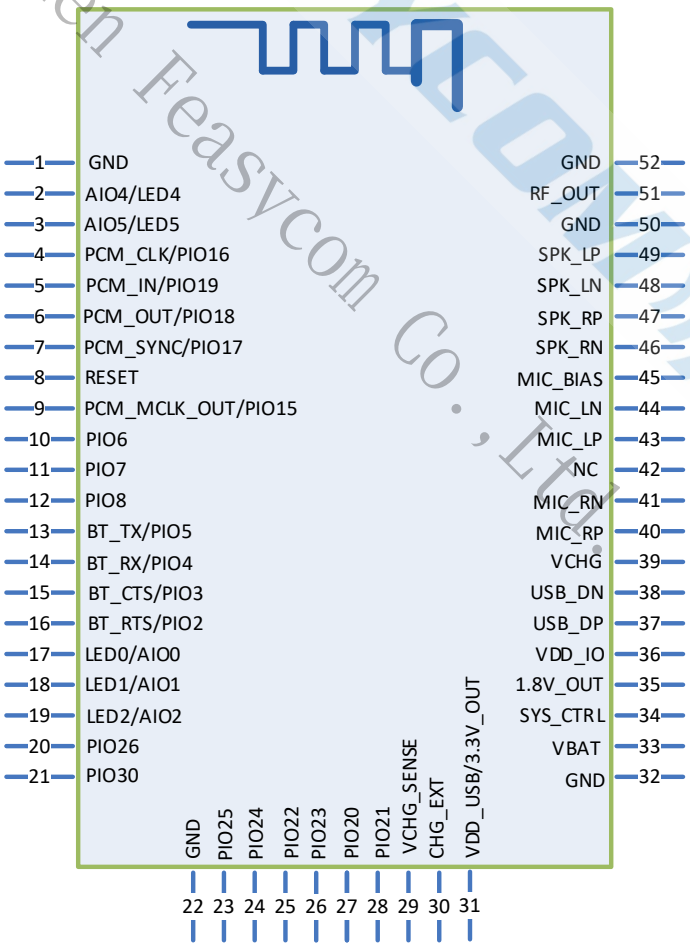

Figure 3-2:FSC-BT1038x PIN Diagram(Top View)

3.2 PIN Definition Descriptions

Table 3-2：Pin definition

Pin	Pin Name	Type	Pin Descriptions	Notes
1	GND	Vss	Power Ground	
2	AIO4/LED4	A,I/O	General-purpose analog/digital input or open drain LED output.	
3	AIO5/LED5	A,I/O	General-purpose analog/digital input or open drain LED output.	
4	PCM_CLK/PIO16	I/O	Programmable I/O line 16. Alternative function: PCM_CLK	
5	PCM_IN/PIO19	I/O	Programmable I/O line 19. Alternative function: PCM_DIN[0]	
6	PCM_OUT/PIO18	I/O	Programmable I/O line 18. Alternative function: PCM_DOUT[0]	
7	PCM_SYNC/PIO17	I/O	Programmable I/O line 17. Alternative function: PCM_SYNC	
8	RESET	I/O	Automatically defaults to RESET# mode when the device is unpowered, or in off modes. Reconfigurable as a PIO after boot.	
9	PCM_MCLK_OUT/PIO15	I/O	Programmable I/O line 15. Alternative function: MCLK_OUT	
10	PIO6	I/O	Programmable I/O line 6. Alternative function: TBR_MOSI[0]	
11	PIO7	I/O	Programmable I/O line 7. Alternative function: TBR_MISO[0]	
12	PIO8	I/O	Programmable I/O line 8. Alternative function: TBR_CLK	
13	BT_TX/PIO5	I/O	BT_TX /Programmable I/O line 5. Alternative function: TBR_MISO[1]	
14	BT_RX/PIO4	I/O	BT_RX/Programmable I/O line 4. Alternative function: TBR_MOSI[1]	
15	BT_CTS/PIO3	I/O	BT_CTS/Programmable I/O line 3	
16	BT_RTS/PIO2	I/O	BT_RTS/Programmable I/O line 2	
17	AIO0/LED0	A,I/O	General-purpose analog/digital input or open drain LED output.	

18	AIO1/LED1	A,I/O	General-purpose analog/digital input or open drain LED output.
19	AIO2/LED2	A,I/O	General-purpose analog/digital input or open drain LED output.
20	PIO26	I/O	Programmable I/O line 26
21	PIO30	I/O	Programmable I/O line 30
22	GND	Vss	Power Ground
23	PIO25	I/O	Programmable I/O line 25
24	PIO24	I/O	Programmable I/O line 24
25	PIO22	I/O	Programmable I/O line 22
26	PIO23	I/O	Programmable I/O line 23
27	PIO20	I/O	Programmable I/O line 20.
28	PIO21	I/O	Programmable I/O line 21.
29	VCHG_SENSE		Charger input sense pin after external mode sense-resistor. High impedance. NOTE: If using internal charger connect VCHG_SENSE direct to VCHG.
30	CHG_EXT		External charger transistor current control. Connect to base of external charger transistor as per application schematic.
31	VDD_USB/3.3V_OUT		3.3V voltage output (MAX. 50mA OUT)
32	GND	Vss	Power Ground
33	VBAT_IN	Vdd	Battery voltage input.
34	SYS_CTRL	I	Typically connected to an ON/OFF push button. Boots device in response to a button press when power is still present from battery and/or charger but software has placed the device in the OFF or DORMANT state. Additionally useable as a digital input in normal operation. No pull.
35	1.8V_OUT	Vdd	1.8V voltage output
36	VDD_IO	I	PIO supply(1.8 V~3.3V)
37	USB_DP		USB Full Speed device D+
38	USB_DN		USB Full Speed device D-
39	VCHG	Vdd	Charger input to Bypass regulator.（USB VBUS）
40	MIC_RP	A	Microphone differential 2 input, positive. Alternative function: Differential audio line input right, positive
41	MIC_RN	A	Microphone differential 2 input, negative. Alternative function: Differential audio line input right, negative
42	NC		
43	MIC_LP	A	Microphone differential 1 input, positive.

			Alternative function: Differential audio line input left, positive
44	MIC_LN	A	Microphone differential 1 input, negative. Alternative function: Differential audio line input left, negative
45	MIC_BIAS	Vdd	Mic bias output.
46	SPK_RN		Differential right line output, negative
47	SPK_RP		Differential right line output, positive
48	SPK_LN	A	Differential left line output, negative
49	SPK_LP	A	Differential left line output, positive
50	GND	Vss	Power Ground
51	RF_OUT	RF	Bluetooth transmit/receive.
52	GND	Vss	Power Ground

4 PHYSICAL INTERFACE

4.1 UART Interface

FSC-BT1038x UART interface is a standard 4-wire interface with RX, TX, CTS, and RTS. Supports H4 HCI interface

or raw UART to application. The default baud rate is 115.2 kbaud. In order to support high and low speed baud rate, FSC-BT1038x provides multiple UART clocks.

The UART signal level ranges from 1.8V to 3.3V. The host provides the power source with the targeted power level to the UART interface via the VIO_HOST pin .

Table 4-1： Possible UART Settings

Parameter	Possible Values
Baudrate	Minimum 1200 baud (≤0%Error)
	Standard 115200bps(≤0.08%Error)
	Maximum 4Mbps(≤0%Error)
Flow control	Supports Automatic Flow Control (CTS and RTS lines)
Parity	None, Odd or Even
Number of stop bits	1
Bits per channel	8

4.2 Standard I²S/PCM Interface (Input only)

FSC-BT1038x provides a standard I²S/PCM interface capable of operating at up to a 384 kHz sample rate.

The I²S/PCM port is highly configurable with alternate PCM modes, and has the following options:

- SYNC edge position selectable to align with start of channel data (PCM mode), or 1 clock before start of channel

data (I²S mode)

- Master (generate CLK and SYNC) or Slave (receive CLK and SYNC) (PCM/I²S)
- SYNC polarity (PCM)
- Long or short SYNC (PCM)
- Left or right justification (PCM/I²S)
- Sign extension / zero pad (PCM)
- Optional tri-state at end of word (PCM)
- Optional invert of clock (PCM/ I²S)
- 13/16/24-bit per sample (PCM/ I²S)
- Up to four slots per frame (PCM)

Table 4-2： PCM and I²S pin and signal names

I²S Pin	PCM function	Description
I²S_SD_IN/SDIN/ADCDAT	PCM_IN	Data intput
I²S_WS/FS/LRCLK	PCM_SYNC	Word sync
I²S_SCK/CLK/BCLK	PCM_CLK	Bit clock

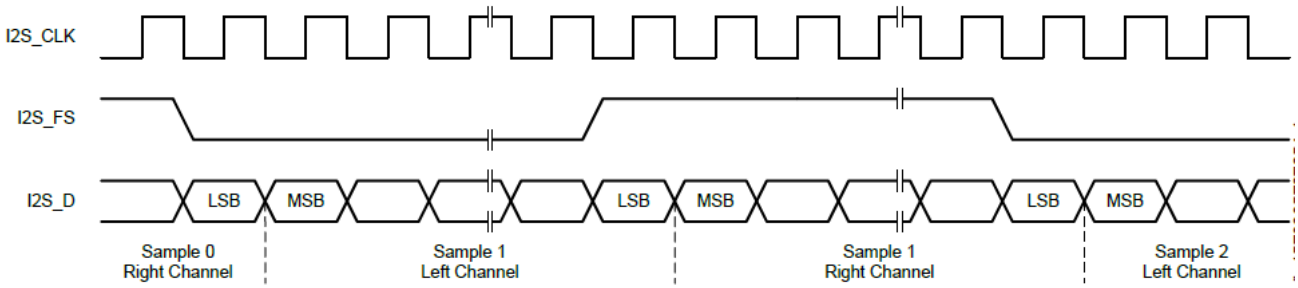

Figure 4-2: I²S general format

4.2.1 I²S/PCM master mode timing diagram

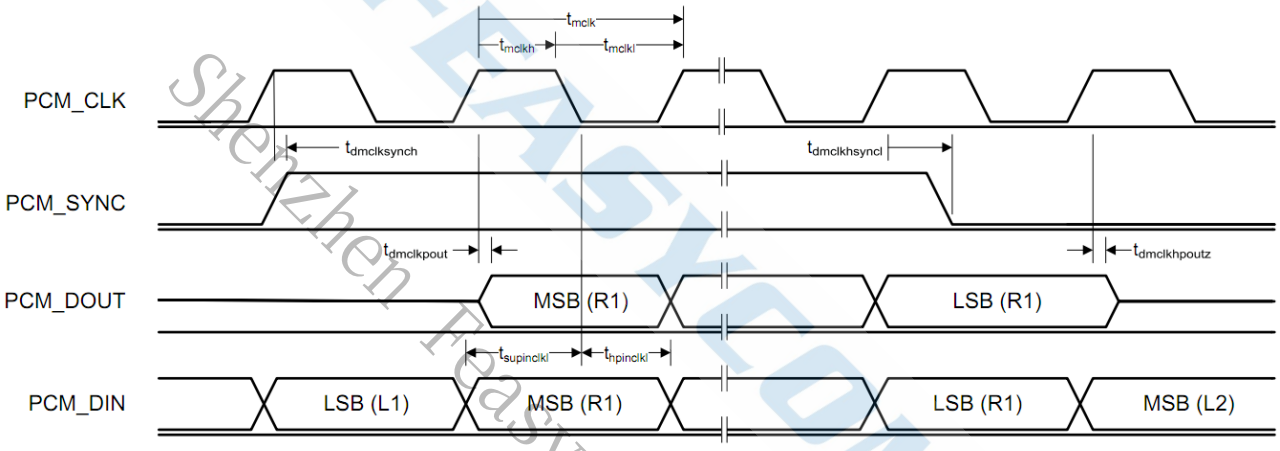

Figure 4-2-1: I²S/PCM master mode timing diagram

NOTE

- Diagram shows I²S standard format, but timing information also applies to PCM mode.
- PCM_DOUT to tri-state is not applicable in I²S mode, because I²S standard requires excess bits to be zero padded.
- With inverted CLK option selected the active CLK edges swap polarity.
- 1/ t_{mclk} is the audio sample frequency. I²S specification requires that t_{mclkh} and t_{mclkl} must be greater than or equal to 0.35 t_{mclk}

Table 4-2-1: I²S/PCM master mode timing diagram symbols

Parameter	Min	Type	Max	Unit
$t_{dmclksynch}$ - Delay time from PCM_CLK high to PCM_SYNC high	-	-	20	ns
$t_{dmclkpout}$- Delay time from PCM_CLK high to valid PCM_OUT	-	-	20	ns
$t_{dmclkhsyncl}$ - Delay time from PCM_CLK high to PCM_SYNC low	-	-	20	ns
$T_{dmclkhpoutz}$- Delay time from PCM_CLK high to PCM_OUT high impedance	-	-	20	ns
$t_{supinclkl}$ - Set-up time for PCM_IN valid to PCM_CLK low	-	-	20	ns
$t_{hpinclkl}$ - Hold time for PCM_CLK low to PCM_IN invalid	0	-	-	ns

4.2.2 I²S/PCM slave mode timing diagram

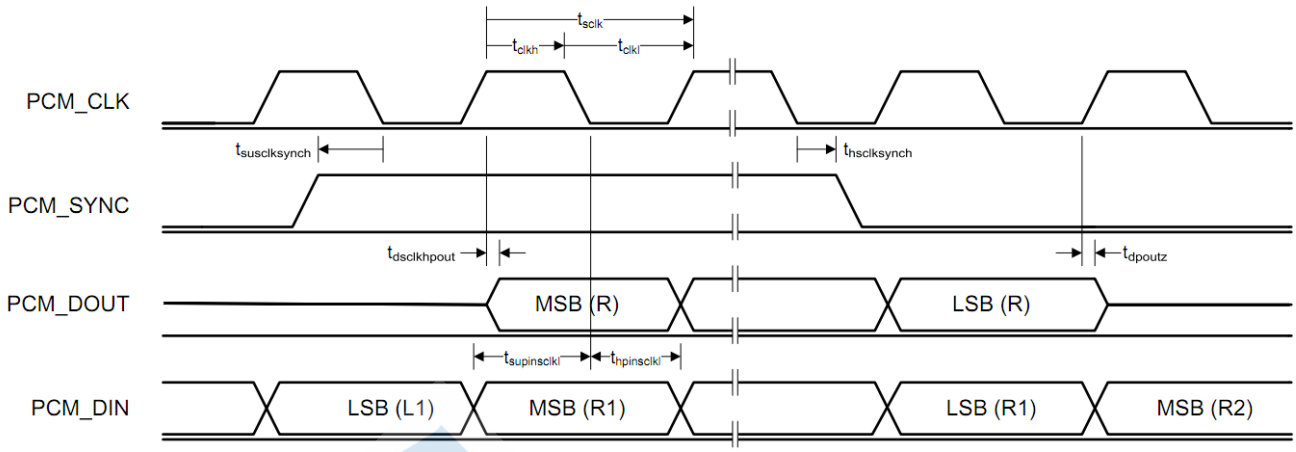

Figure 4-2-2: I²S/PCM slave mode timing diagram

NOTE

- Diagram shows I²S standard format, but timing information also applies to PCM mode.
- PCM_DOUT to tri-state is not applicable in I²S mode, because I²S standard requires excess bits to be zero padded.
- With inverted CLK option selected the active CLK edges swap polarity.
- 1/ t_{sclk} is the audio sample frequency. I²S specification requires that t_{sclkh} and t_{sclkl} must be greater than or equal to 0.35 t_{sclk}

Table 4-22: I²S/PCM slave mode timing diagram symbols

Parameter	Min	Type	Max	Unit
$t_{hsclksynch}$ - Hold time from PCM_CLK low to PCM_SYNC high	5	-	-	ns
$t_{susclksynch}$ - Set-up time for PCM_SYNC high to PCM_CLK low	15	-	-	ns
$t_{dsclkhpout}$- Delay time from PCM_CLK high to PCM_OUT valid data	-	-	20	ns
t_{dpoutz}- Delay time from PCM_CLK high to PCM_OUT data line high impedance	-	-	20	ns
$t_{supinsclkl}$ - Set-up time for PCM_IN valid to PCM_CLK low	15	-	-	ns
$t_{hpinsclkl}$ - Hold time for PCM_CLK low to PCM_IN invalid	5	-	-	ns

4.3 Analog audio Interfaces

4.3.1 Line/mic input

FSC-BT1038x has two high-quality audio input ADCs (HQADC), primarily intended for line input use, but also suitable for other applications that support mixed differential and single ended use cases. The ADC is 24-bit, and capable of sample rates from 8 kHz to 96 kHz. The HQADC is configurable, with an internal switch arrangement, see Figure 9. VAG is a virtual ground reference. The software API allows for direct control of the nine switches, or a simpler control, supporting three standard modes:

- Stereo differential input
- Stereo single ended input, using the P inputs
- Stereo single ended input, using the N inputs

Inputs should be AC coupled, typically with a 2u2 capacitor. This capacitor value can be reduced at the expense of low frequency response attenuation.

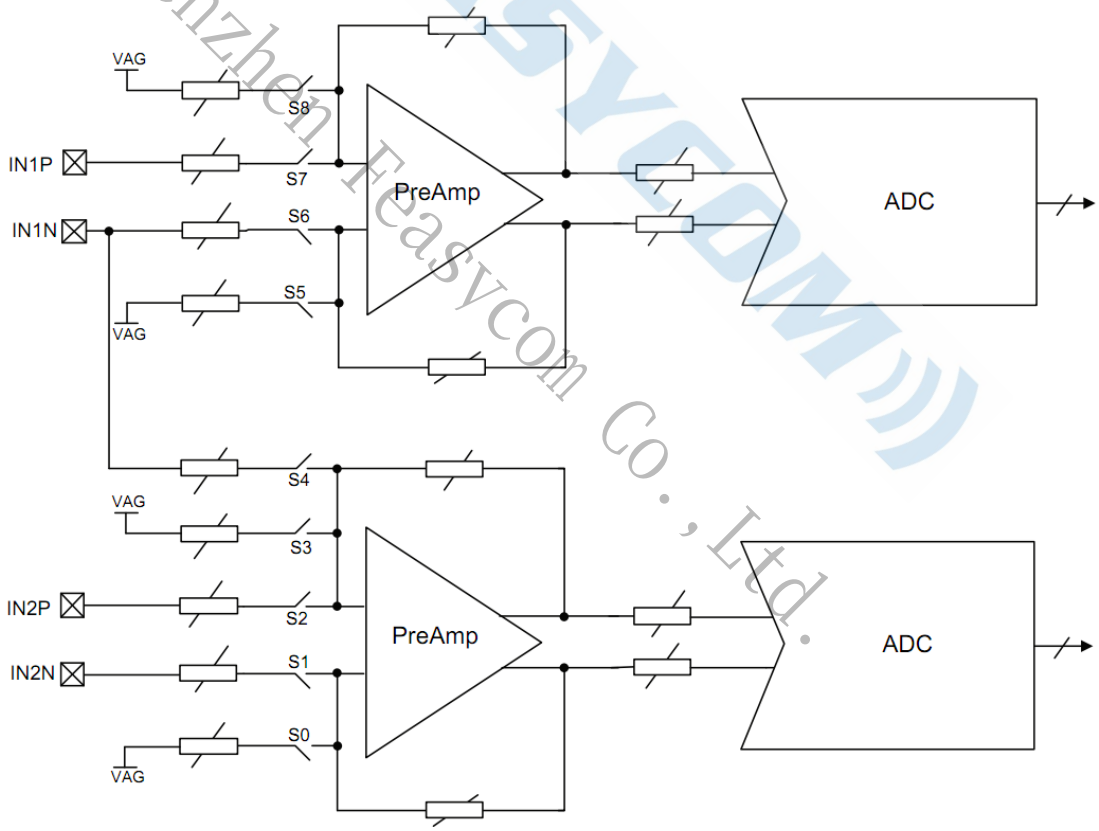

Figure 4-3-1: high-quality ADC input switch configuration

4.4 USB Interfaces

- FSC-BT1038x has a USB device interface: An upstream port, for connection to a host Phone/PC
- The device port is a USB2.0 Full Speed (12 Mb/s) port. Typically FSC-BT1038x enumerates as a compound device with a hub with the enabled audio source / sink / HID / mass storage device appearing behind this hub.
- The DP 1.5 k pull-up is integrated in FSC-BT1038x. No series resistors are required on the USB data lines.
- FSC-BT1038x contains integrated ESD protection on the data lines to IEC 61000-4-2 (device level). In normal applications, no external ESD protection is required.
- Extra ESD protection is not required on VCHG (VBUS) because FSC-BT1038x meets the USB certification requirements of a minimum of 1uF, and a maximum of 10 µF being present on VCHG (VBUS).
- The VCHG input of FSC-BT1038x is tolerant of a constant 6.5 V and transients up to 7.0 V. If extra overvoltage protection is required, external clamping protection devices can be used.
- FSC-BT1038x supports charger detection to the USB BCv1.2 standard.
- Updater and RF testing

4.5 Programming and Debug Interfaces

FSC-BT1038x provides a debug (Pin10~12) interface for programming, updata，configuring, and debugging the FSC-BT1038x.

4.6 Standard PIO

The standard digital I/O pins (PIO) on FSC-BT1038x are split into separate pad domains. Each VDD_IO

domain can be separately powered, from 1.7 V to 3.3 V. When PIOs in a supply domain are used for a high-speed interface, decoupling the respective VDD_IO pin with a 100 nF decoupling capacitor may be beneficial. The

VDD_IO of a particular pin should be powered before voltages are applied to any PIO powered by that domain, otherwise back powering can occur through the electrostatic discharge (ESD) protection in the pad.

PIO can be programmed to have a pull-up or pull down with two strengths (weak and strong). PIO can also be

programmed with a sticky function where they are strongly pulled to their current input state. PIO have a reset pull state, after reset the pulls can be re-configured by software.

PIO also have a programmable drive strength capability of 2, 4, 8, or 12 mA.

All PIO are readable by all subsystems, but for write access are assigned by software to particular subsystem

control. PIO inputs are via Schmitt triggers.

4.7 SYS_CTRL pin

- SYS_CTRL is an input pin that acts as a power on signal for the internal regulators.
- From the OFF state, SYS_CTRL must be asserted for >20 ms to start power up.
- SYS_CTRL is VBAT tolerant (4.8 V max), and typically connected via a button to VBAT. SYS_CTRL has no internal pull resistor, and requires an external pull-down if left undriven.

- Use software to logically disconnect SYS_CTRL from the power on signal for internal regulators. For example, when booted, software takes control of the internal regulators and the state of SYS_CTRL is ignored by the regulators.

4.8 Reset pin

FSC-BT1038x is digital reset pin (RESET#) is an active low reset signal.

The pin is active low and on-chip glitch filtering avoids the need to filter out any spurious noise that may cause unintended resets. The RESET# pin has a fixed strong pull-up to VDD_IO, and therefore can be left unconnected. The input is asynchronous, and is pulse extended within FSC-BT1038x to ensure a full reset

FSC-BT1038x contains internal Reset Protection functionality to automatically keep the power rails enabled and enable the system to restart after unintended reset (such as a severe ESD event). Assertion of RESET# beyond the Reset Protection timeout (typically greater than ~1.8 s) causes the device to power down if VCHG is not present and SYS_CTRL is low. FSC-BT1038x then requires a SYS_CTRL assertion or VCHG attach to restart.

NOTE

- FSC-BT1038x is always powered if VCHG is present. It does not power down if RESET# is asserted while VCHG remains present.
- FSC-BT1038x is powered down via software-controlled methods rather than external assertion of RESET#.
- Holding RESET# low continuously is not the lowest FSC-BT1038x power state, because pull downs are enabled on VCHG and VDD_USB in this state.
- RESET# is guaranteed to work if held low for 120 µs

4.9 LED Drivers

- LED Driver: This mode is designed for driving LEDs. The pad operates as an open-drain pad, tolerable of voltages up to 7.0 V. Therefore the cathode of the LED should be connected to the FSC-BT1038x LED pad. Each pad is rated to sink up to 50 mA of current.
- FSC-BT1038x has five PWM-based LED controllers controlled by the Applications subsystem. Use them for driving either the LED pads (through virtual PIOs) or other available PIOs.
- An application may configure the LED flash rate and ramp time using a dedicated API.
- Once configured, the LED flash and ramp rate are fully hardware controlled within the LED/PWM module. It is possible to synchronize any number of the LED drivers together. Use the flash/ramp rate configuration to generate color change sequences on RGB LEDs.

5 ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

All measurements are referenced at the module pins unless otherwise indicated. All specifications are over process and voltage unless otherwise indicated.

Over operating free-air temperature range (unless otherwise noted)

Table 5-1：Absolute Maximum Rating

Parameter	Min	Type	Max	Unit
VCHG	-0.4		6.5	V
VBAT_IN	-0.4		4.8	V
VDD_IO	-0.4		3.8	V
Digital I/O	-0.4		3.8	
VDD_USB/3.3_OUT	-0.4		3.8	V
LED/AIO	-0.4		+7/2.1	V
1.8V_OUT/MIC_BIAS	-0.4		2.1	V
Storage temperature (T_{stg})	-40		85	°C

5.2 Recommended Operating Conditions

Table 5-2：Recommended Operating Conditions

Parameter	Min	Type	Max	Unit
VCHG	4.75	5.0	6.5	V
VBAT_IN	3.0	3.3	4.2	V
VDD_IO	1.8	3.3	3.6	V
Digital I/O	0	3.3	3.6	
VDD_USB/3.3_OUT*	2.8		3.5	V
LED/AIO	0		6.5/1.95	V
1.8V_OUT/MIC_BIAS	1.7		1.95	V
Operating temperature (T_A)	-40		85	°C

* 1, When the Pin33(BAT_IN) with a 3V0~4V2 , this pin outputs 2V8 ~ 3V0

2, when the No. 39 PIN (VCHG) with a 5V input pin, this pin outputs 3.2V ~ 3.5V

6 MSL & ESD

Table 6-1: MSL and ESD

Parameter	Value
MSL grade:	MSL 3
ESD grade	Electrostatic discharge
ESD – Human-body model (HBM) rating, JS-001-2017 (Total samples from one wafer lot)	Pass ±2000 V
ESD – Charge-device model (CDM) rating, JS-002-2018 (Total samples from one wafer lot)	Pass ±500 V

7 RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccate (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the below and follow instructions specified by IPC/JEDEC J-STD-033.

Note: The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the below , the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccate and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60%RH.

Notice (注意) :

Feasycom module must use Step-Stencil, suggestion using the stencil thickness about 0.16-0.2mm,it could be modify with the product.

Table 7-1: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Feasycom surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

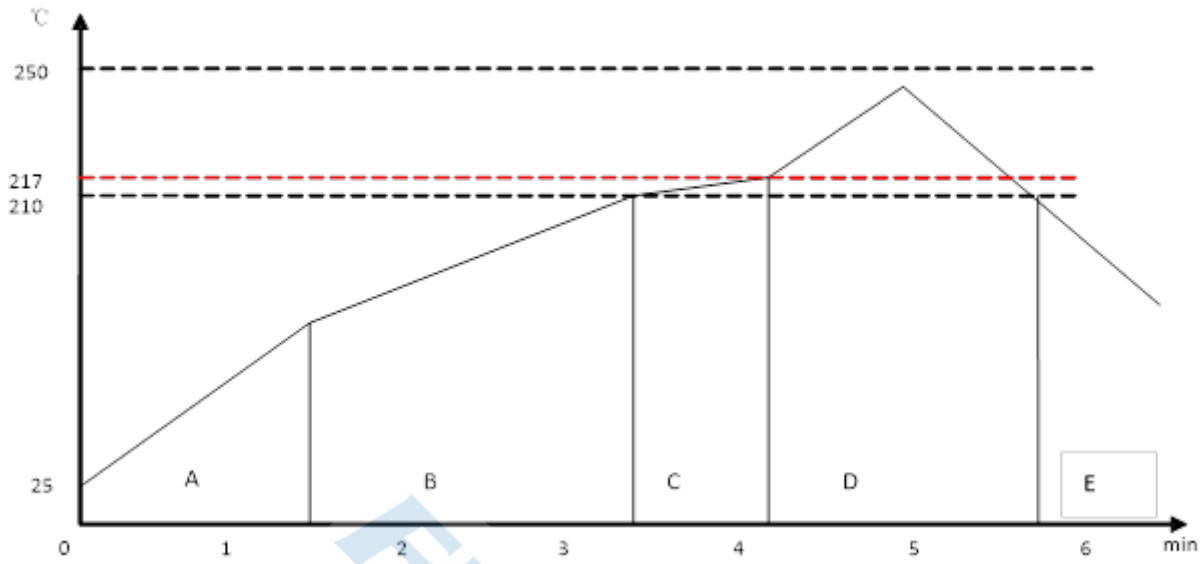

Figure 7-1：Typical Lead-free Re-flow

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

Equilibrium Zone 2 (C) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

8 MECHANICAL DETAILS

8.1 Mechanical Details

- Dimension: 13mm(W) x 26.9mm(L) x 2.2mm(H) Tolerance: ±0.2mm
- Module size: 13mm X 26.9mm Tolerance: ±0.2mm
- Pad size: 1.6mmX0.6mm Tolerance: ±0.2mm
- Pad pitch: 1.0mm Tolerance: ±0.1mm
- **(Residual plate edge error: < 0.5mm)**

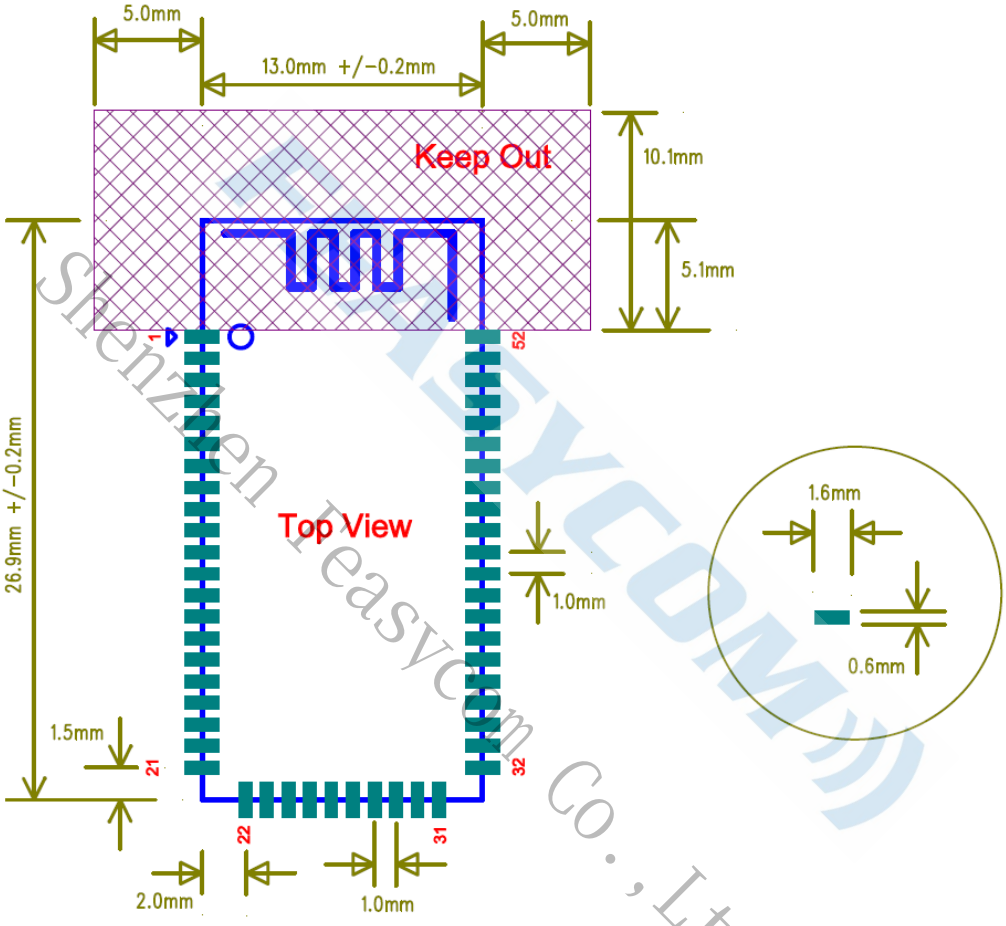

Figure 8-1：FSC-BT1038x footprint Layout Guide (Top View)

9 HARDWARE INTEGRATION SUGGESTIONS

9.1 Soldering Recommendations

FSC-BT1038x is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

9.2 Layout Guidelines(Internal Antenna)

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.

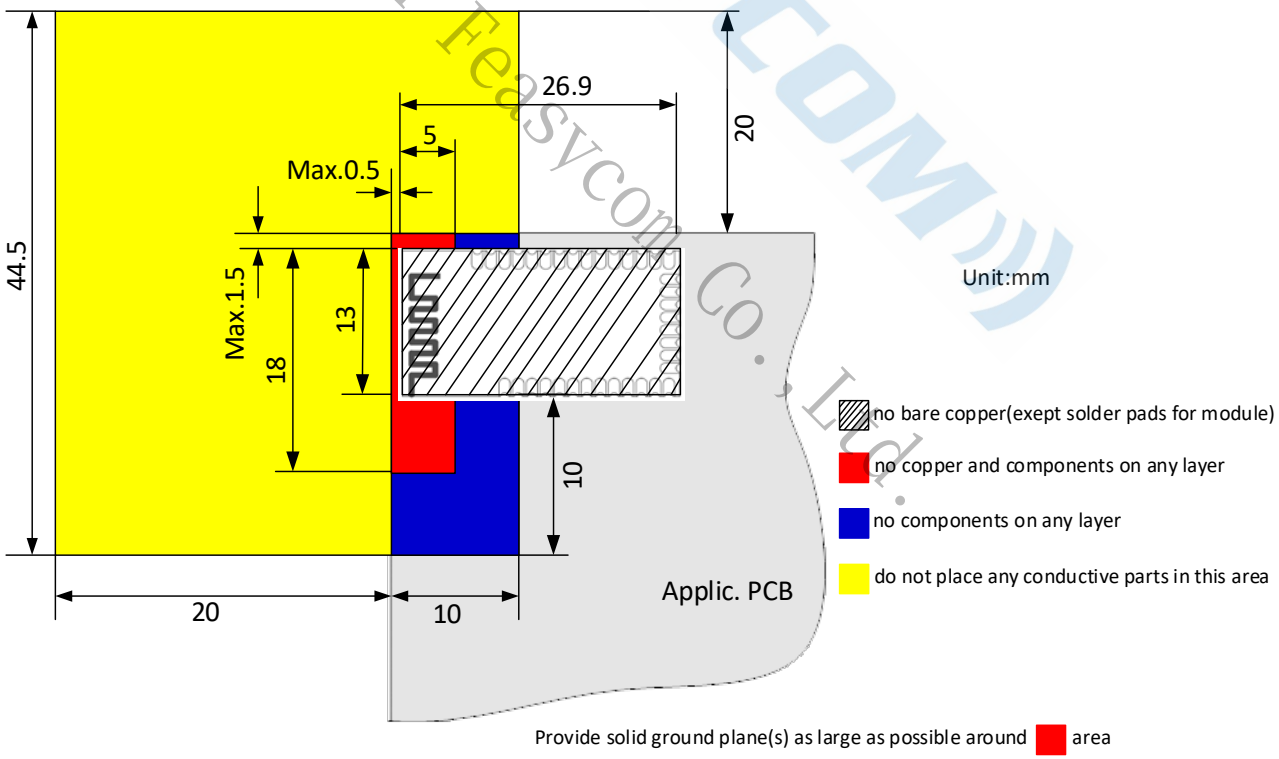

Figure 9-2: Restricted Area (Design schematic, for reference only. Unit: mm)

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid

problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

9.3 Layout Guidelines(External Antenna)

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

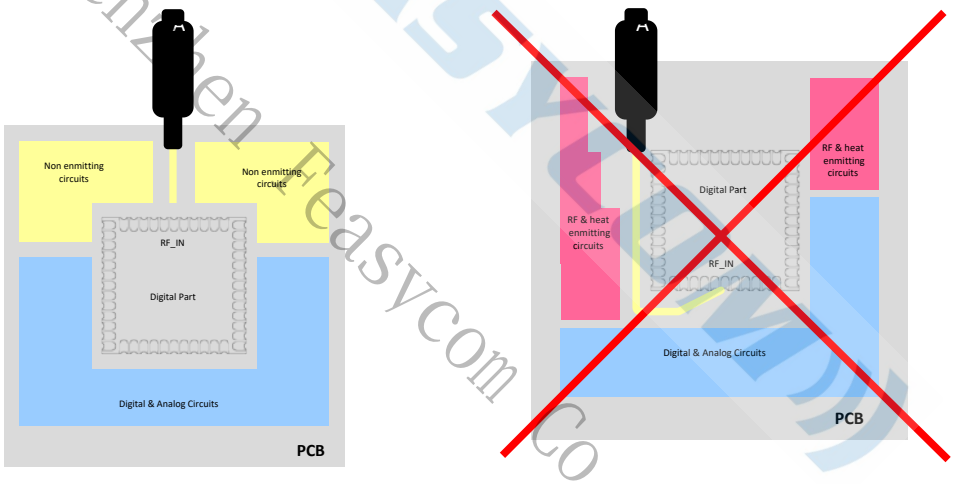

Figure 9-3: Placement the Module on a System Board

9.3.1 Antenna Connection and Grounding Plane Design

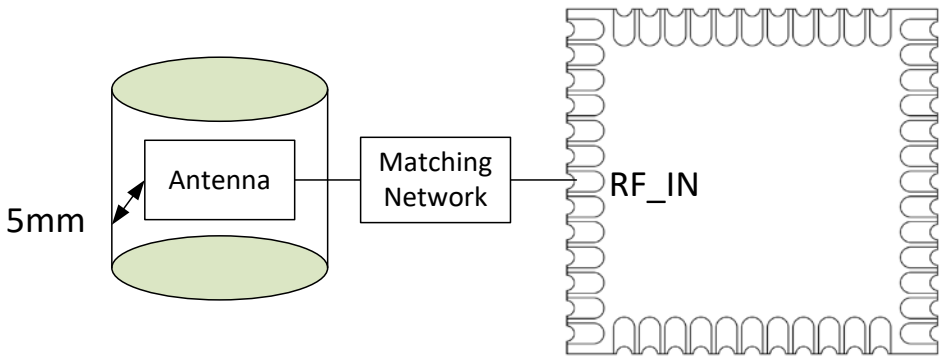

Figure 9-31-0: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

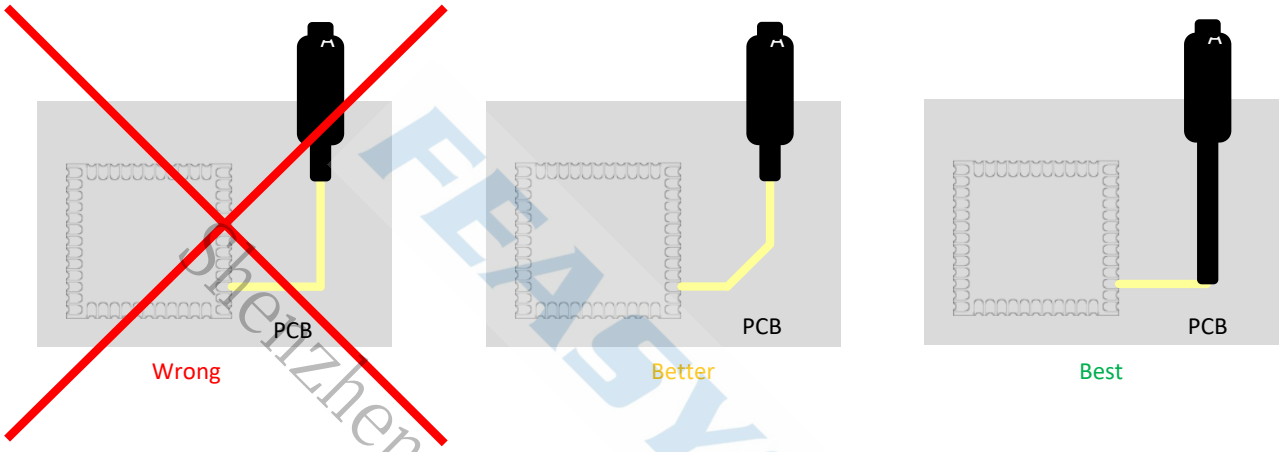

Figure 9-31-1: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

10 PRODUCT PACKAGING INFORMATION

10.1 Default Packing

Figure 10-1: Tray Dimension: 140mm * 265mm Tray vacuum

10.2 Packing box(Optional)

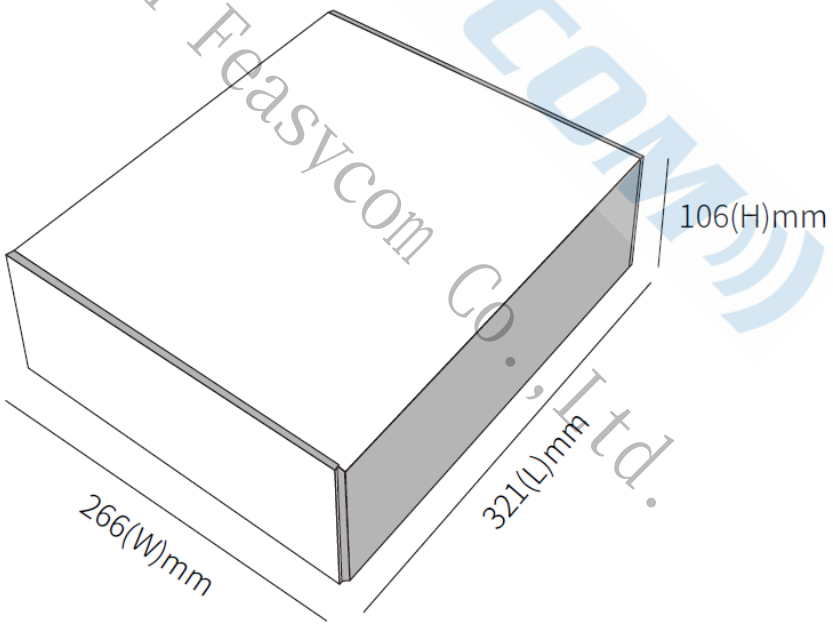

Figure 10-2: Packing box(Optional)

** If other packing is required, please confirm with the customer*

** Packing: 1000pcs per carton (Minimum packing quantity)*

** The outer packing size is for reference only, please refer to the actual size*

11 APPLICATION SCHEMATIC