

FSC-BW3581A

Wi-Fi 6 2.4G&5G+BT 5.4 module Datasheet V1.1



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Version	Data	Notes	Writer
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1.INTRODUCTION

Overview

FSC-BW3581A is a highly integrated module with dual band Wi-Fi 6 and BT 5.4 for wireless application.

Wi-Fi 6 Features

- CMOS single-chip fully-integrated RF, Modem and MAC
- Support 2.4G/5GHz Wi-Fi 6
- Data rates up to 600Mbps with 20/40/80MHz bandwidth
- Support 5MHz/10MHz mode
- RX sensitivity -92dBm in 11b 1M mode
- Tx power up to 21dBm in 11b mode, 18dBm in HT/VHT/HE MCS0 mode
- Support STA, AP, Wi-Fi Direct modes concurrently
- Support STBC, beamforming, Wi-Fi6 TWT
- Support WEP/WPA/WPA2/WPA3-SAE Personal, MFP

BT 5.4 Features

- Supports all the mandatory and optional features of Bluetooth 2.1+EDR/3.0/4.x/5.3/5.4
- Supports advanced master and slave topologies

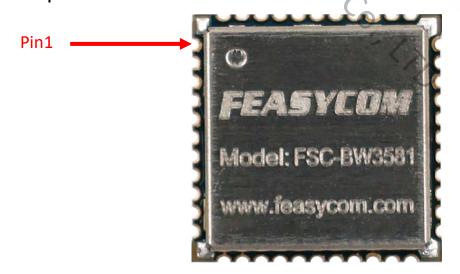
Other Features

- Supports SDIO3.0/USB2.0/HCI UART/PCM interface
- Integrated low power timer and watchdog

Applications

- IoT devices
- Wireless devices

Module picture



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1.1 Selection of version

Table 1-1: Selection of version

Order Number	Descriptions	Module picture as below showing
FSC-BW3581A (One antenna, default) (-40°C ~+85°C)	PIN No.2 RF_IO_ Wi-Fi /BT: 2.4GHz Wi-Fi & BT + 5GHz Wi-Fi PIN No.4 NC External antenna(stamp hole, PIN No.2)	FEASYLUM Model: FSC-BW3531 www.feasycom.com
FSC-BW3581A (Two antennas, default) (-40°C ~+85°C)	PIN No.2 2.4GHz + 5GHz Wi-Fi PIN No.4 BT Two external antennas must be soldered (stamp hole, PIN No.2 and PIN No.4)	FEASYCOM Model: FSC-BW3531 www.feasycom.com
See chapter 3.3 for details	s	

2.General Specifications

Table 2-2: General Specifications

Categories	Features	Implementation
Bluetooth	7	
	Bluetooth Standard	Bluetooth V5.4
	Frequency Band	2402MHz~2480MHz
	Bluetooth class	Class 1
	Transmit power	10dBm@ enhance data rate 14dBm@ basic rate 14dBm@ low energy
	Receiver sensitivity	-92dBm @ enhance data rate -92dBm @ basic rate -92dBm @ low energy
	Support mode	Slave and Master
	Profiles	HFP, A2DP, AVRCP, SPP, PBAP, HID, DUN, FTP, GATT, IAP2, ANCS
	Maximum throughput	2Mbps
	Interface	UART/PCM
Wi-Fi		
	Wi-Fi standard	2.4G: IEEE802.11 b/g/n/ac/ax 5G: IEEE802.11 a/n/ac/ax
	Frequency Band	2.400 GHz ~ 2.4835 GHz (2.4 GHz ISM Band) 5.150 GHz ~ 5.850 GHz (5.0 GHz Band)
	Frequency Tolerance	≦ ±20ppm

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	2.4G Output Power	802.11b /11Mbps: 21dBm ± 2 dB 802.11g /54Mbps: 17dBm ± 2 dB 802.11n /MCS0: 18dBm ± 2 dB 802.11n /MCS7: 16dBm ± 2 dB 802.11n /MCS11: 13dBm ± 2 dB 802.11ac /MCS0: 18dBm ± 2 dB 802.11ac /MCS11: 13dBm ± 2 dB 802.11ac /MCS11: 13dBm ± 2 dB 802.11ax /MCS0: 18dBm ± 2 dB 802.11ax /MCS0: 18dBm ± 2 dB	EVM≤-9dB EVM≤-25dB EVM≤-10dB EVM≤-28dB EVM≤-35dB EVM≤-35dB EVM≤-15dB EVM≤-35dB EVM≤-35dB
	5G Output Power	802.11a /54Mbps: 17dBm ± 2 dB 802.11n /MCS0: 18dBm ± 2 dB 802.11n /MCS7: 16dBm ± 2 dB 802.11n /MCS11: 13dBm ± 2 dB 802.11ac /MCS0: 18dBm ± 2 dB 802.11ac /MCS11: 13dBm ± 2 dB 802.11ax /MCS0: 18dBm ± 2 dB 802.11ax /MCS0: 18dBm ± 2 dB	EVM≤-25dB EVM≤-10dB EVM≤-28dB EVM≤-35dB EVM≤-35dB EVM≤-35dB EVM≤-35dB EVM≤-35dB
	2.4G Rx Sensitivity	-95dBm @11b 1M -87dBm @11b 11M -92dBm @11g 6M -76dBm @11g 54M -92dBm @HT20 MCS0 -89dBm @HT40 MCS0 -91dBm @HE20 MCS0 -65dBm @HE20 MCS11 -88dBm @HE40 MCS0 -62dBm @HE40 MCS11	
	5G Rx Sensitivity	-92dBm @6M bps OFDM -75dBm @54M bps OFDM -92dBm @HT20 MCS0 -89dBm @HT40 MCS0 -90dBm @HE20 MCS0 -63dBm @HE20 MCS11 -87dBm @HE40 MCS0 -60dBm @HE40 MCS11 -83dBm @HE80 MCS11	
Security		WEP/WPA/WPA2/WPA3-SAE	
Interface		SDIO	
Size		12mm(L) x 12mm(W) x 2.2mm(H)	

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FSC-BW3581A Datasheet



Hardware Interface		UART, GPIO, PCM,USB
Antenna		External Dual-band antenna, supporting 2.4GHz and 5.8GHz frequencies
Operating temperature		-40°C ~ +85°C
Storage temperature		-40°C ~ +85°C
Operating voltage (VBAT)		3.0~3.6V (Peak Current:1.5A)
VIO		1.8V or 3.3V
Miscellaneous	Lead Free	Lead-free and RoHS compliant
Wilderianeous	Warranty	One Year
Humidity		10% ~ 90% non-condensing
MSL grade:		MSL 3
ESD grade:	Sh	Human Body Model: Pass ±3000 V, all pins Charge device model: Pass ±800 V, all pins
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3. Diagram

3.1 Block Diagram

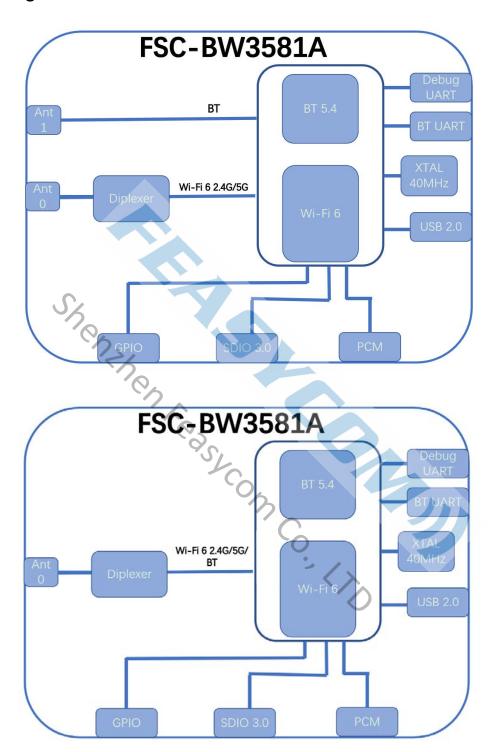


Figure 3-1: FSC-BW3581A Block Diagram

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3.2 Pin Diagram

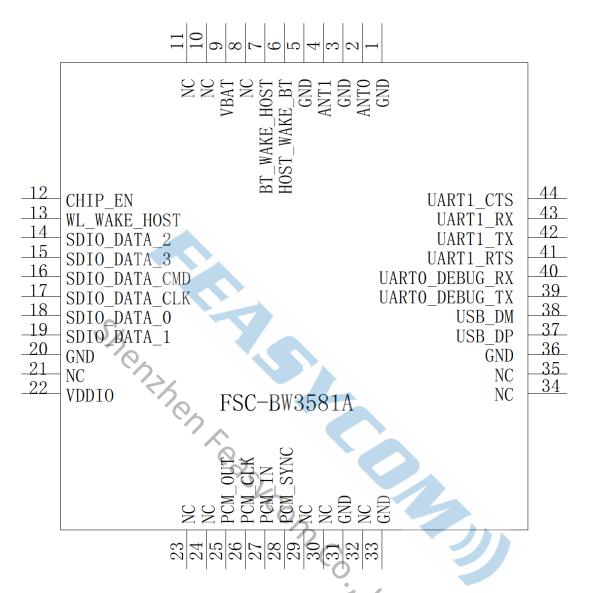


Figure3-2:FSC-BW3581A Pin Diagram(Top View)

3.3 Pin Definition Descriptions

Table 3-3: Pin definitions

Pin	Pin Name	Туре	Pin Descriptions	Notes
1	GND		Ground connections	
2	ANT0	RF	Wi-Fi and BT antenna(optional)	
3	GND		Ground connections	
4	ANT1	PF	BT antenna(optional)	
5	GND		Ground connections	
6	HOST_WAKE_BT	1	HOST wake-up Bluetooth device	
7	BT _WAKE_HOST	0	Bluetooth device to wake-up HOST	
8	NC			

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10 NC 11 NC 12 CHIP_EN I Enable /unable BT and WIFI 13 WL_WAKE_HOST O WLAN to wake-up HOST 14 SDIO_D2 I/O SDIO Data Line2 15 SDIO_D3 I/O SDIO Command Input 16 SDIO_CLK I SDIO Clock Input 18 SDIO_D0 I/O SDIO Data Line1 19 SDIO_D1 I/O SDIO Data Line1 20 GRD Ground connections 21 NC I/O SUBJO Data Line1 22 VDDIO PWR 1.8V or 3.3V Supply Voltage 23 NC I/O PCM output signal 24 NC I/O PCM output signal 25 PCM OUT O PCM output signal 26 PCM SYNC I/O PCM synchronization signal 27 PCM IN PCM synchronization signal 28 PCM SYNC I/O PCM synchronization signal 30 <th>9</th> <th>VBAT</th> <th>PWR</th> <th>3.3V Supply Voltage</th>	9	VBAT	PWR	3.3V Supply Voltage
12	10	NC		
13	11	NC		
14 SDIO_D2	12	CHIP_EN	I	Enable /unable BT and WIFI
15 SDIO_D3	13	WL_WAKE _HOST	0	WLAN to wake-up HOST
16 SDIO_CMD I/O SDIO Command Input 17 SDIO_CLK I SDIO Clock Input 18 SDIO_D0 I/O SDIO Data Line0 19 SDIO_D1 I/O SDIO Data Line1 20 GND Ground connections 21 NC I/O 22 VDDIO PWR 1.8V or 3.3V Supply Voltage 23 NC I/O 24 NC I/O 25 PCM OUT O PCM output signal 26 PCM CLK I/O PCM clock signal 27 PCM IN PCM input signal 28 PCM SYNC I/O PCM synchronization signal 29 NC I/O PCM synchronization signal 30 NC I/O PCM synchronization signal 31 GND Ground connections 32 NC I/O 33 GND Ground connections 34 NC I/O 35 <td< td=""><td>14</td><td>SDIO_D2</td><td>I/O</td><td>SDIO Data Line2</td></td<>	14	SDIO_D2	I/O	SDIO Data Line2
17 SDIO_CLK I SDIO_Clock Input 18 SDIO_D0 I/O SDIO Data Line0 19 SDIO_D1 I/O SDIO Data Line1 20 GND Ground connections 21 NC I/O PCM CLK 22 VDDIO PWR 1.8V or 3.3V Supply Voltage 23 NC I/O PCM output Signal 24 NC I/O PCM output Signal 26 PCM CLK I/O PCM synchronization signal 27 PCM IN PCM synchronization signal 28 PCM SYNC I/O PCM synchronization signal 29 NC I/O PCM synchronization signal 30 NC I/O PCM synchronization signal 31 GND Ground connections 32 NC I/O I/O 33 GND Ground connections 34 NC I/O USB Data D+ 35 NC I/O USB Data D+ <t< td=""><td>15</td><td>SDIO_D3</td><td>I/O</td><td>SDIO Data Line3</td></t<>	15	SDIO_D3	I/O	SDIO Data Line3
18	16	SDIO_CMD	I/O	SDIO Command Input
19	17	SDIO_CLK	ı	SDIO Clock Input
20 GND Ground connections 21 NC 22 VDDIO PWR 1.8V or 3.3V Supply Voltage 23 NC 24 NC 25 PCM OUT O PCM output signal 26 PCM CLK I/O PCM clock signal 27 PCM IN PCM input signal 28 PCM SYNC I/O PCM synchronization signal 29 NC 30 NC 31 GND Ground connections 32 NC 33 GND Ground connections 34 NC 35 NC 36 GND Ground connections 37 USB_DP I/O USB Data D+ 39 UARTO_Debug_TX I/O Debug serial port Tx 40 UARTO_Debug_RX I/O Debug serial port Rx Hang in the air when not in use, no need to connect 41 UART1_RTS O High speed UART Data Out	18	SDIO_D0	I/O	SDIO Data Line0
21	19	SDIO_D1	1/0	SDIO Data Line1
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PCM OUT O PCM output signal PCM CLK I/O PCM clock signal PCM IN PCM input signal PCM SYNC I/O PCM synchronization signal PCM S	22	VDDIO	PWR	1.8V or 3.3V Supply Voltage
PCM OUT O PCM output signal PCM CLK VO PCM clock signal PCM IN PCM input signal PCM SYNC I/O PCM synchronization SIGNAL PCM SYNCHIA SY	23	NC		
26 PCM CLK I/O PCM clock signal 27 PCM IN PCM input signal 28 PCM SYNC I/O PCM synchronization signal 29 NC 30 NC 30 NC 31 GND Ground connections 32 NC 33 GND Ground connections 34 NC 35 NC 36 GND Ground connections 37 USB_DP I/O USB Data D+ 38 USB_DM I/O USB Data D- 39 UART0_Debug_TX I/O Debug serial port Tx Hang in the air when not in use, no need to connect 40 UART0_Debug_RX I/O Debug serial port Rx Hang in the air when not in use, no need to connect 41 UART1_RTS O High speed UART RTS 42 UART1_TX O High speed UART Data Out 43 UART1_RX I High speed UART Data In	24	NC S		
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PCM SYNC I/O PCM synchronization signal PCM Synchronizati	26	PCM CLK	I/O	PCM clock signal
29 NC 30 NC 31 GND Ground connections 32 NC 33 GND Ground connections 34 NC 35 NC 36 GND Ground connections 37 USB_DP I/O USB Data D+ 38 USB_DM I/O USB Data D- 39 UARTO_Debug_TX I/O Debug serial port Tx Hang in the air when not in use, no need to connect 40 UART1_RTS O High speed UART RTS 42 UART1_TX O High speed UART Data Out 43 UART1_RX I High speed UART Data In	27	PCM IN	10	PCM input signal
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Hang in the air when not in use, no need to connect UARTO_Debug_RX I/O Debug serial port Rx Hang in the air when not in use, no need to connect UART1_RTS O High speed UART RTS UART1_TX O High speed UART Data Out High speed UART Data In	38	USB_DM	I/O	USB Data D-
40 UARTO_Debug_RX I/O Hang in the air when not in use, no need to connect 41 UART1_RTS O High speed UART RTS 42 UART1_TX O High speed UART Data Out 43 UART1_RX I High speed UART Data In	39	UARTO_Debug_TX	I/O	
42 UART1_TX O High speed UART Data Out 43 UART1_RX I High speed UART Data In	40	UARTO_Debug_RX	I/O	
43 UART1_RX I High speed UART Data In	41	UART1_RTS	0	High speed UART RTS
	42	UART1_TX	0	High speed UART Data Out
44 UART1_CTS I High speed UART CTS	43	UART1_RX	I	High speed UART Data In
	44	UART1_CTS	I	High speed UART CTS

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4 ELECTRICAL CHARACTERISTICS

4.1 DC Characteristics

Table 4-1: Power Supply Characteristics

Parameter	Min	Туре	Max	Unit
Operating Temperature	-40	25	85	°C
VDD_3V3	3.0	3.3	3.6	V
VDD_IO	1.62	1.8 or 3.3	3.6	V

4.2 Power Supply DC Characteristics

Table 4-2: Power Consumption

Symbol	Parameter	Туре	Unit
Power Consumption	WiFi unssociated	48	mA
	2.4G WiFi TRX Throughput(BT Disable)	310	mA
	5G WiFi TRX Throughput(BT Disable)	360	mA
	2.4G WiFi TRX Throughput(Bluetooth playback of music)	318	mA
	5G WiFi TRX Throughput(Bluetooth playback of music)	390	mA
	2.4G Tx@MCS7/18dbm	138	mA
	2.4G Rx@11b 1M	46	mA
	5G Tx@MCS7/18dbm	154	mA
	5G Rx@11a 6M	58	mA
	BT Tx(13dbm,1M)	60	mA
	BT Rx	57	mA

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5 PHYSICAL INTERFACE

5.1 System Power on Sequence

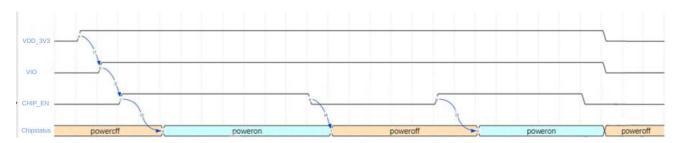


Figure 5-1: System Power on Sequence

t1: VIO's power on time >= VDD_3V3's

t2: CHIP_EN's high time >= VIO's +200us

t3: chip all power on ready time >= CHIP_EN high time + 8ms

t4:CHIP_EN pull low to chip all power off time >=6ms

5.2 UART Interface

The four signal pins facilitate the UART function. When connecting the FSC-BW3581A to another digital device, UART_RX and UART_TX enable data transmission between the two devices. The other two pins, UART_CTS and UART_RTS, support RS232 hardware flow control. Both pins operate on a low-level effective basis, allowing transmission when the signal is low and halting transmission when the signal is high.

When connecting the module to a host, please make sure to follow.

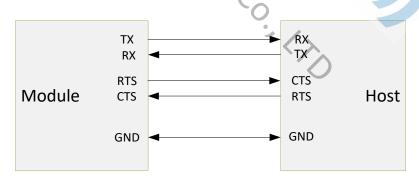


Figure 5-2: UART Connection

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6 MSL&ESD

Table 6-1: MSL and ESD

Parameter	Value
MSL grade:	MSL 3
ESD grade	Electrostatic discharge
ESD – Human Body Model (HBM) Rating JESD22-A114-B	Pass ±3000 V, all pins
ESD – Charged Device Model (CDM) Rating JESD22-C101-D	Pass ±800 V, all pins

7. RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to reflow, it is crucial to ensure that the modules are properly packaged to prevent moisture absorption. The new packages are equipped with desiccants to absorb moisture, and a humidity indicator card is included to indicate the moisture level maintained during storage and shipment. If the card indicates the need to bake the units, please refer to the instructions specified by IPC/JEDEC J-STD-033 and follow them accordingly. It is important to adhere to these instructions to prevent any potential moisture-related issues during the reflow process.

Note: The shipping tray should not be exposed to temperatures exceeding 65°C. If baking is necessary at higher temperatures indicated below, it is essential to remove the modules from the shipping tray. This precaution is important to avoid any potential damage or deformation to the tray caused by excessive heat.

Any module that exceeds its floor life but has not yet been manufactured should be repackaged by using new desiccants and humidity indicator cards. For devices with a Moisture Sensitivity Level (MSL) of 3, the floor life is 168 hours in an environment with 30°C/60%RH.

Floor life refers to the maximum allowable time a moisture-sensitive device can be exposed to ambient conditions without risking moisture absorption and potential damage during soldering.

Notice:

The Feasycom's module must be used with a Step-Stencil. It is suggested to use a stencil thickness of approximately 0.16-0.2mm, which can be modified according to the product.

使用我司模块,须使用阶梯钢网,建议阶梯钢网厚度0.16-0.20mm,可根据自己产品适应性,进行相应调整.

Table 7-1: Recommended baking times and temperatures

	125°C Ba	king Temp.	90°C/≤ 5%RH Baking Temp		40°C/ ≤ 5%RH Baking Temp.	
MSL	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

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Feasycom surface mount modules are designed to facilitate easy manufacturing, including reflow soldering onto a PCB. However, it is the customer's responsibility to select the suitable solder paste and ensure that the oven temperatures during reflow meet the requirements specified by the solder paste manufacturer. Feasycom surface mount modules comply with the J-STD-020D1 standards for reflow temperatures.

The soldering profile may vary depending on different parameters, requiring a specific setup for each application. The data provided here is only intended as a general guideline for solder reflow and should be used as a reference.

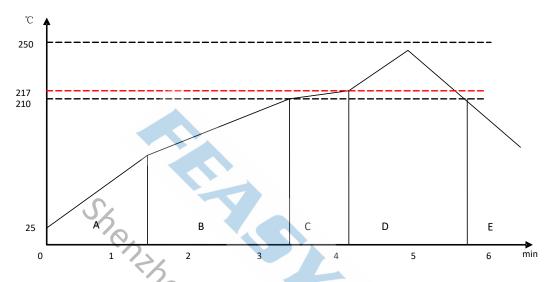


Figure 7-1: Typical Lead-free Re-flow

Pre-heat zone (A) — This zone gradually increases the temperature at a controlled rate, usually **ranging from 0.5 to 2 °C/s**. Its purpose is to preheat the PCB board and components to a temperature of 120-150 °C. This stage is necessary to ensure the even distribution of heat across the PCB board and to remove any remaining solvents completely, minimizing the risk of heat shock to the components.

Equilibrium Zone 1 (B) — In this stage, the flux undergoes softening and uniformly covers the solder particles, as well as spreading over the PCB board. This process helps prevent re-oxidation of the solder particles. Additionally, as the temperature rises and the flux liquefies, each activator and rosin component become activated. They work together to eliminate any oxide film formed on the surface of the solder particles and PCB board. **For this zone, it is recommended to maintain a temperature range of 150 to 210 °C for a duration of 60 to 120 seconds.**

Equilibrium Zone 2 (C) (optional) — To address the issue of upright components, it is recommended to maintain a temperature range of 210 to 217 °C for a duration of approximately 20 to 30 seconds. This will help ensure proper soldering and alignment of the components on the PCB board.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is $230 \sim 250 \, ^{\circ}$ C. The soldering time should be 30 to 90 second when the temperature is above $217 \, ^{\circ}$ C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4** °C.

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8.MECHANICAL DETAILS

Mechanical Details

Dimension: 12mm(W) x 12mm(L) x 2.2mm(H) Tolerance: ±0.2mm

Module size: 12.00mm X 12.00mm Tolerance: ±0.2mm
 Pad size: 1.7mm X 0.5mm Tolerance: ±0.1mm

• Pad pitch: 0.9mm Tolerance: ±0.1mm

(分板后边角残留板边误差:不大于 0.5mm) (Residual plate edge error after panel separation:< 0.5mm)

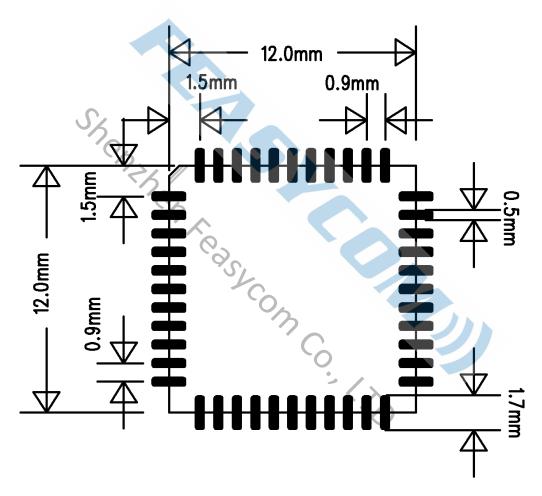


Figure 8-1: FSC-BW3581 footprint Layout Guide (Top View)

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9. Layout Guideline

9.1 SDIO Lines Layout Guideline

The following SDIO line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive 8mA.

SDIO_DATA_CMD_WL
SDIO_DATA_CLK_WL
SDIO_DATA_0_WL
SDIO_DATA_3_WL

The route length of these signals be less than 15 cm and the line impedance be less than 50Ω

9.2 HCI Lines Layout Guideline

The following HCI line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive $4 \sim 8mA$

UART1_RX

UART1 TX

UART1 CTS

UART1_RTS

The route length of these signals be less than 15 cm and the line impedance be less than 50Ω

9.3 Power Trace Lines Layout Guideline

VDD 3V3 Trace Width: 40mil

VDD_IO Trace Width: 20mil

9.4 Ground Lines Layout Guideline

A Complete Ground in Ground Layer.

Add Ground Through Holes to FSC-BW3581A Module Ground Pads

Decoupling Capacitors close to FSC-BW3581A Module Power and Ground Pads

9.5 Antenna Layout Guideline

The placement and PCB layout play a critical role in optimizing the performance of modules without on-board antenna designs. The trace connecting the antenna port of the module to an external antenna should have a characteristic impedance of 50Ω and should be kept as short as possible to prevent interference into the transceiver of the module. When positioning the external antenna and RF-IN port of the module, it is important to keep them away from any sources of noise and digital traces. To minimize return loss and achieve better impedance matching, a matching network may be required between the external antenna and RF-IN port.

To ensure proper RF performance, it is recommended to clearly separate the RF critical circuits of the module from any digital circuits on the system board. The RF circuits within the module are located near the antenna port. Therefore, the module should be placed in such a way that the module's digital part faces the digital section of the

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system PCB.

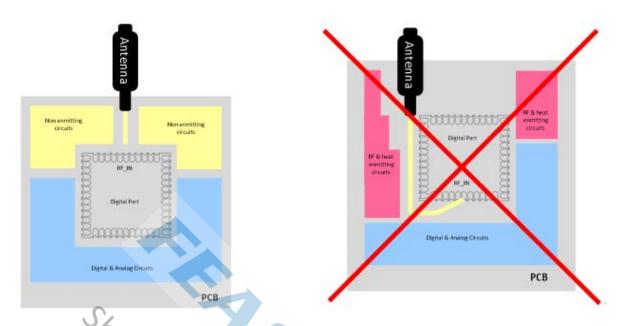


Figure 9-5: Placement the Module on a System Board

9.6 Antenna Connection and Grounding Plane Design

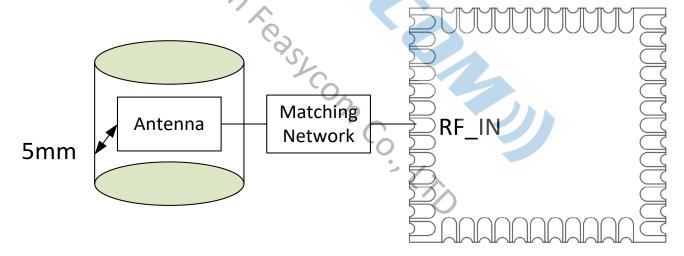


Figure 9-6-1: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should be at least as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.

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• To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

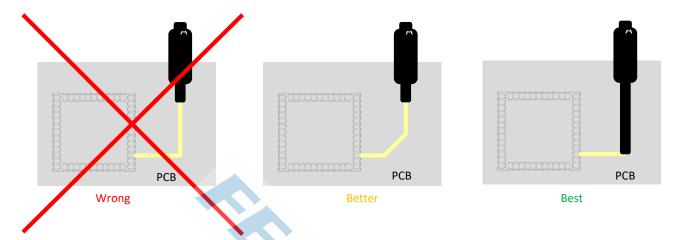


Figure 9-6-2: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip
 line to the ground plane on the bottom side of the receiver is very small and has huge tolerances.
 Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

10. PRODUCT PACKAGING INFORMATION

10.1 Default Packing

a, Tray vacuum

b, Tray Dimension: 150mm * 150mm

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Figure 10-1: Tray vacuum

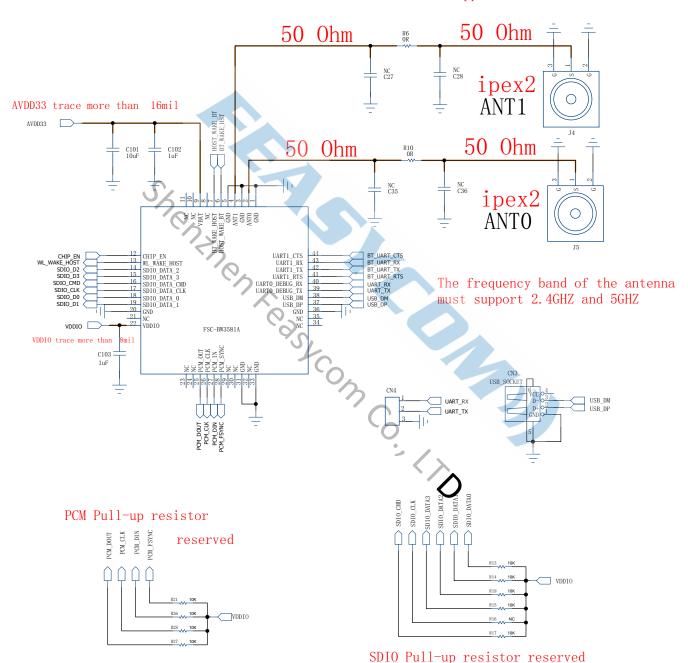
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11.APPLICATION SCHEMATIC

AVDD33 peak current 1.5A

The frequency band of the antenna must support 2.4GHZ



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