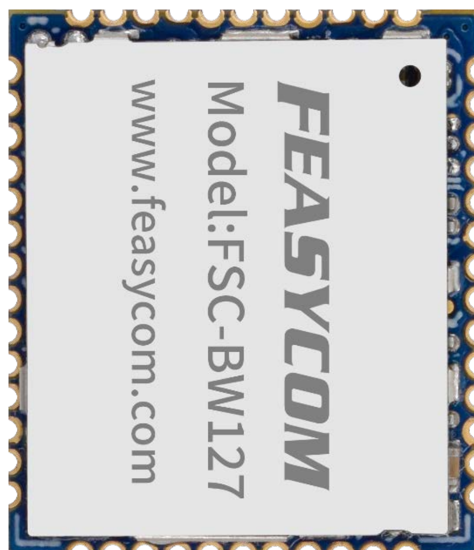

FSC-BW127

DATASHEET V1.1

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Revision History

Version	Data	Notes	Author
V1.0	2023-06-20	Initial Version	Devin Wan
V1.1	2023-06-25	Update Image of Module, Add product model: FSC-BW127B.	Devin Wan

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Contact Us

Shenzhen Feasycom Co.,LTD

Email: sales@feasycom.com

Address: Rm 508, Building A, Fenghuang Zhigu, No.50, Tiezai Road, Xixiang, Baoan District,Shenzhen,518100,China.
Tel: 86-755-27924639

1 INTRODUCTION

Overview

FSC-BW127 is a low-cost and low-power consumption module which has all of the Wi-Fi functionalities. It is a highly-integrated IEEE 802.11 a/b/g/n/ac/ax MAC/Baseband/RF WLAN single chip. For Wireless LAN operation. The integrated module provides SDIO 3.0 interface for Wi-Fi. The module provides simple legacy and 20MHz/40MHz/80MHz co-existence mechanism to ensure backward and network compatibility.

The wireless module complies with IEEE 802.11 a/b/g/n/ac/ax 2x2 MIMO standard and the speed can achieve up to 1201Mbps with dual stream in 802.11ax. The integrated module provides SDIO interface for Wi-Fi, UART / PCM interface for Bluetooth.

This combo module is a total solution for a combination of Wi-Fi and Bluetooth V5.2 technologies. The module is specifically developed for all portable devices.

Therefore, FSC-BW127 provides an ideal solution for developers who want to integrate Wi-Fi & Bluetooth wireless technology into their design.

General Features

- Highly integrated wireless local area network (WLAN) system-on-chip (SOC) for 802.11a/b/g/n/ac/ax WLAN applications

Backward compatible with 802.11a/n/ac devices while operating at 802.11ax data rates.

- Support 802.11ax 2x2, with OFDMA and MU-MIMO, by 4 types PPDU format, such as HE-SU-PPDU, HE-ER-SU-PPDU, HEMU-PPDU, and HE-TB-PPDU.
- Complete 802.11n MIMO solution for 2.4GHz and 5Ghz band
- Maximum PHY data rate up to 286.8 Mbps using 20MHz bandwidth, 573.5Mbps using 40MHz bandwidth, and 1201Mbps using 80MHz bandwidth
- Backward compatible with 802.11a/b/g devices while operating at 802.11n data rates
- Backward compatible with 802.11a/n/ac devices while operating at 802.11ax data rates

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Host Interface

- Complies with SDIO 1.1/2.0/3.0 for WLAN with clock rate up to 208MHz.
- Complies with HS-UART with configurable baud rate for Bluetooth.

Bluetooth Features

- Supports Bluetooth 5.2 system (BT5.2 Logo Compliant)
- Supports WLAN/Bluetooth coexistence
- Compatible with Bluetooth v2.1+EDR.
- Dual Mode support: Simultaneous LE and BR/EDR
- BT host digital interface: HCI UART & PCM for audio data

PHY Features

- IEEE 802.11ax MIMO OFDM /OFDMA
- IEEE 802.11ac MIMO OFDM
- IEEE 802.11n MIMO OFDM
- Two Transmit and Two Receive paths
- 20MHz / 40MHz / 80MHz bandwidth transmission
- Support 2.4Ghz and 5Ghz band channels
- DSSS with DBPSK and DQPSK, CCK modulation with long and short preamble
- OFDM with BPSK, QPSK, 16QAM, 64QAM and 256QAM and 1024QAM modulation. Convolutional Coding Rate: 1/2, 2/3, 3/4, and 5/6
- Maximum data rate 54Mbps in 802.11g, 300Mbps in 802.11n and 866.7Mbps in 802.11ac, 1201Mbps in 802.11ax.
- OFDM/DSSS/CCK receive diversity with MRC using up to 2 receive paths.
- Support STBC
- Support LDPC
- Maximum-Likelihood Detection (MLD)
- Fast receiver Automatic Gain Control (AGC)

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Application

- Audio and video system
- Measurement systems
- PND

2 General Specification

Table 2-1：General Specifications

Categories	Features	Implementation
Bluetooth		
	Bluetooth Standard	Bluetooth V5.2
	Frequency Band	2402MHz ~ 2480MHz
	Interface	UART/PCM
	Modulation	GFSK, π /4-DQPSK, 8-DPSK
	Transmit Power	+8 dBm (Max.)
	Receiver	-92dBm (Min.)
Wi-Fi 2.4GHz		

	Item	Specification	EVM
	WLAN Standard	IEEE 802.11 b/g/n/ac/ax Wi-Fi compliant	
	Frequency Range	2.400 GHz ~ 2.497 GHz (2.4 GHz ISM Band)	
	Number of Channels	2.4GHz： Ch1 ~ Ch14	
	Interface	SDIO	
	Output Power	802.11b /11Mbps : 19dBm±2 dB 802.11g /54Mbps : 18dBm±2 dB 802.11n /MCS7 : 17dBm±2 dB 802.11ac vHT20 MCS8: 16dBm±2 dB 802.11ac vHT40 MCS9: 15dBm±2 dB 802.11ax HE20 MCS11: 13dBm±2 dB 802.11ax HE40 MCS11: 13dBm±2 dB	EVM≤-10dB EVM≤-25dB EVM≤-28dB EVM≤-30dB EVM≤-32dB EVM≤-35dB EVM≤-35dB
	SISO Receive Sensitivity (11b,20MHz) @8% PER	1Mbps PER @ -94 dBm 11Mbps PER @ -85 dBm	EVM≤-83dB EVM≤-76dB
	SISO Receive Sensitivity (11g,20MHz) @10% PER	6Mbps PER @ -90 dBm 54Mbps PER @ -71 dBm	EVM≤-85dB EVM≤-68dB
	SISO Receive Sensitivity (11n,20MHz) @10% PER	MCS=0 PER @ -90 dBm MCS=7 PER @ -69 dBm	EVM≤-85dB EVM≤-67dB
	SISO Receive Sensitivity (11n,40MHz) @10% PER	MCS=0 PER @ -87 dBm MCS=7 PER @ -66 dBm	EVM≤-82dB EVM≤-64dB
	SISO Receive Sensitivity (11ac,20MHz) @10% PER	MCS=0 PER @ -90 dBm MCS=8 PER @ -66 dBm	EVM≤-82dB EVM≤-60dB
	SISO Receive Sensitivity (11ac ,40MHz) @10% PER	MCS=0 PER @ -87 dBm MCS=9 PER @ -59 dBm	EVM≤-79dB EVM≤-55dB
	SISO Receive Sensitivity (11ax,20MHz) @10% PER	MCS=0 PER @ -90 dBm MCS=11 PER @ -60 dBm	EVM≤-74dB EVM≤-52dB
	SISO Receive Sensitivity (11ax ,40MHz) @10% PER	MCS=0 PER @ -87 dBm MCS=11 PER @ -57 dBm	EVM≤-71dB EVM≤-49dB
Wi-Fi 5GHz			
	WLAN Standard	IEEE 802.11a/n/ac/ax, Wi-Fi compliant	
	Frequency Range	5.15 GHz ~ 5.850 GHz (5.0 GHz ISM Band)	
	Interface	SDIO	
	Output Power	802.11a /54Mbps : 18dBm±2 dB 802.11n /MCS7 : 17dBm±2 dB 802.11ac vHT20 MCS8: 16dBm±2 dB 802.11ac vHT40 MCS9: 15dBm±2 dB 802.11ac vHT80 MCS9: 15dBm±2 dB 802.11ax HE20 MCS11: 13dBm±2 dB 802.11ax HE40 MCS11: 13dBm±2 dB 802.11ax HE80 MCS11: 13dBm±2 dB	EVM≤-25dB EVM≤-28dB EVM≤-30dB EVM≤-32dB EVM≤-32dB EVM≤-35dB EVM≤-35dB EVM≤-35dB
	SISO Receive Sensitivity (11a,20MHz) @10% PER	6Mbps PER @ -90 dBm 54Mbps PER @ -71 dBm	EVM≤-85dB EVM≤-68dB
	SISO Receive Sensitivity	MCS=0 PER @ -90 dBm	EVM≤-85dB

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	(11n,20MHz) @10% PER	MCS=7 PER @ -69 dBm	EVM≤-67dB
	SISO Receive Sensitivity (11n,40MHz) @10% PER	MCS=0 PER @ -87 dBm MCS=7 PER @ -66 dBm	EVM≤-82dB EVM≤-64dB
	SISO Receive Sensitivity (11ac,20MHz) @10% PER	MCS=0, NSS1 PER @ -90 dBm MCS=8, NSS1 PER @ -66 dBm	EVM≤-82dB EVM≤-60dB
	SISO Receive Sensitivity (11ac ,40MHz) @10% PER	MCS=0, NSS1 PER @ -87 dBm MCS=9, NSS1 PER @ -59 dBm	EVM≤-79dB EVM≤-55dB
	SISO Receive Sensitivity (11ac ,80MHz) @10% PER	MCS=0, NSS1 PER @ -84 dBm MCS=9, NSS1 PER @ -56 dBm	EVM≤-79dB EVM≤-54dB
	SISO Receive Sensitivity (11ax,20MHz) @10% PER	MCS=0 PER @ -90 dBm MCS=11 PER @ -60 dBm	EVM≤-74dB EVM≤-52dB
	SISO Receive Sensitivity (11ax ,40MHz) @10% PER	MCS=0 PER @ -87 dBm MCS=11 PER @ -57 dBm	EVM≤-71dB EVM≤-49dB
	SISO Receive Sensitivity (11ax ,80MHz) @10% PER	MCS=0 PER @ -84 dBm MCS=11 PER @ -54 dBm	EVM≤-68dB EVM≤-46dB
Size	W x L x H	13mm × 15 mm × 2.2mm (Height including shielding case) 13mm × 15 mm × 1.8mm (Height excluding shielding case)	
Operating temperature		0°C ~ +70°C	
Storage temperature		-40°C ~ +85°C	
Supply Voltage		3.0V~3.6V (Peak Current:1.5A)	
VDD_IO		1.7V~3.6V (Peak Current:200mA)	
Miscellaneous	Lead Free Warranty	Lead-free and RoHS compliant One Year	
Humidity		10% ~ 90% non-condensing	
MSL grade:		MSL 3	
ESD grade:		Human Body Model: Pass ±2000 V, all pins Charge device model: Pass ±250 V, all pins	

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3 HARDWARE SPECIFICATION

3.1 Block Diagram and PIN Diagram

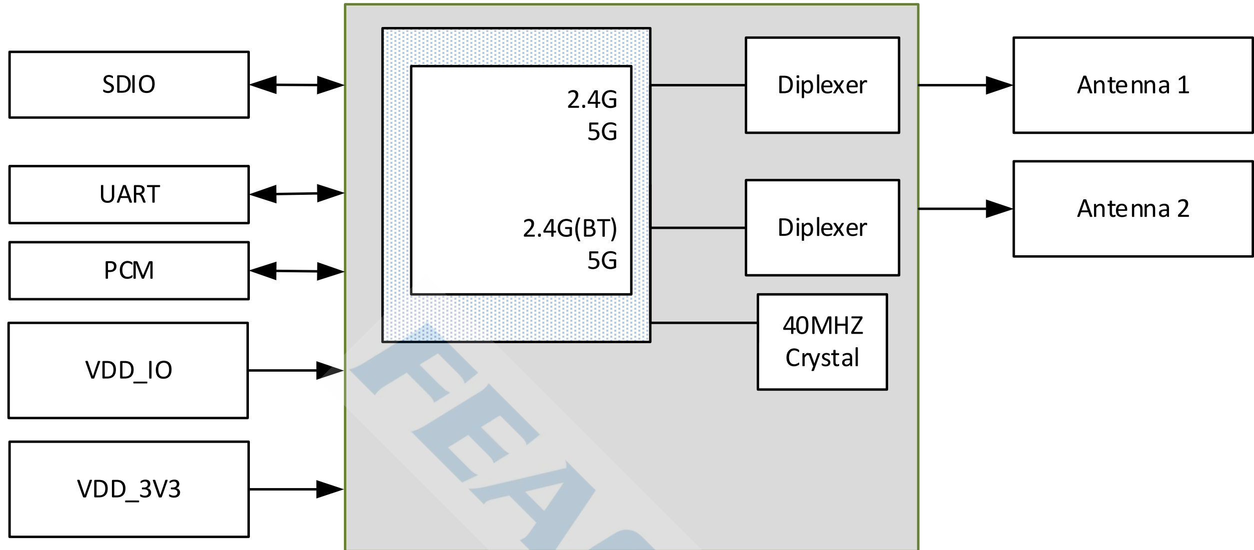

Figure 3-1-1: FSC-BW127 Block Diagram

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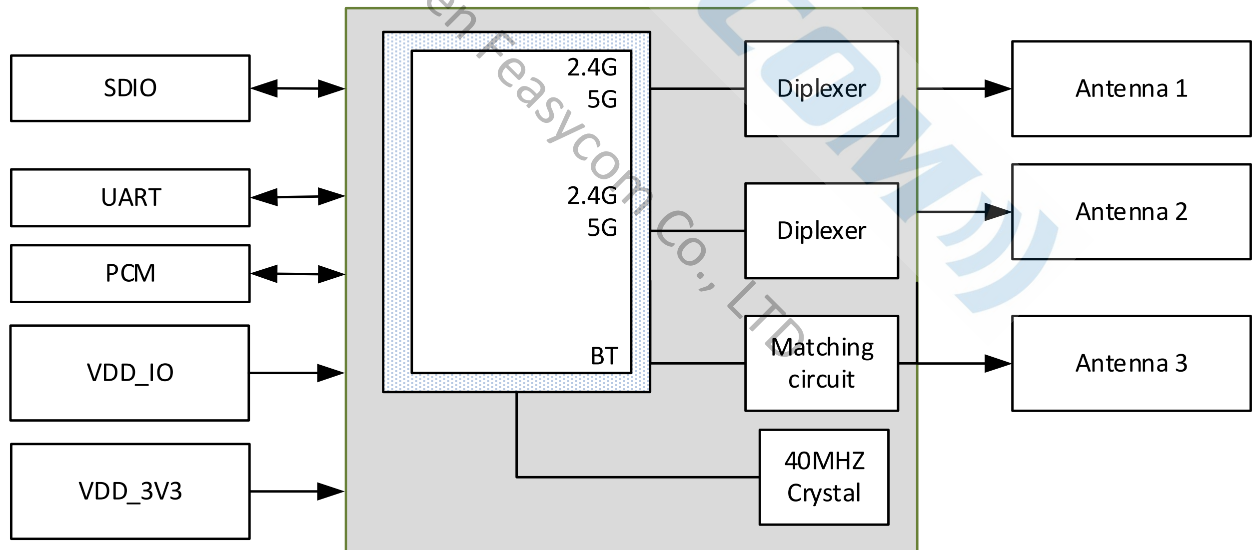

Figure 3-2-2: FSC-BW127B Block Diagram

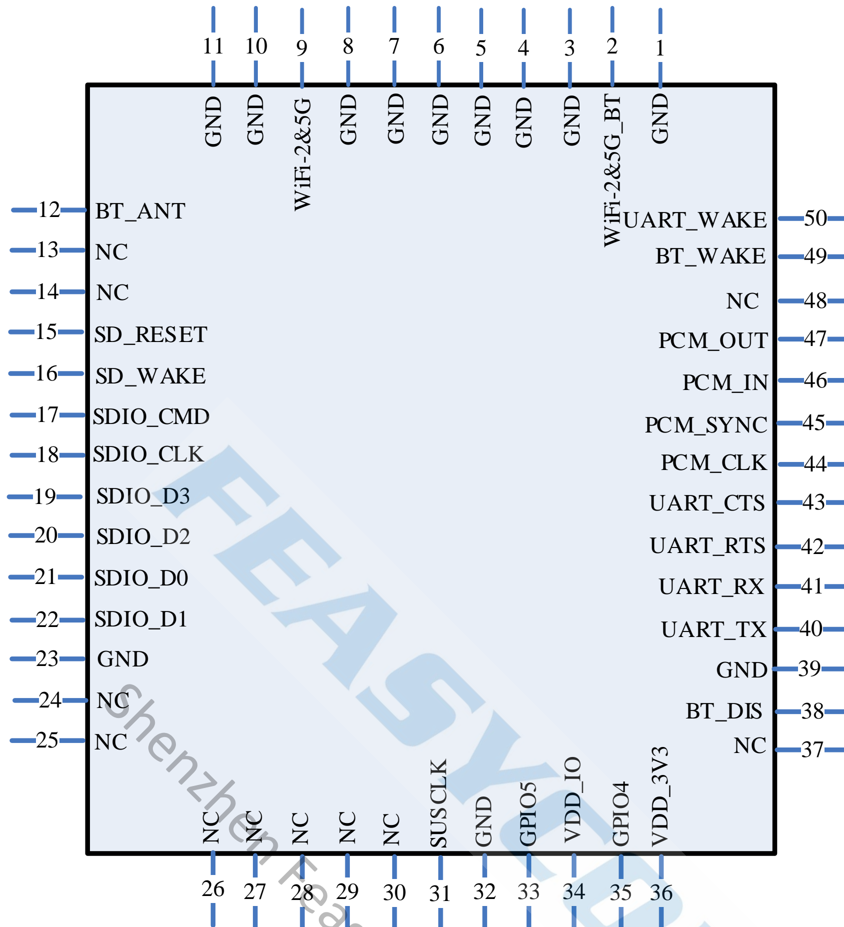

Figure 3-1-3: FSC-BW127 PIN Diagram (Top View)

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3.2 PIN Definition Descriptions

Table 3-2：Pin definition

Pin	Pin Name	Type	Pin Descriptions	Notes
1	GND	Vss	Power Ground	
2	WiFi-2&5G_BT	O	RF I/O port chain1, Wi-Fi 2.4G & 5G, BT 2.4G ***(FSC-BW127 only)*** RF I/O port chain1, Wi-Fi 2.4G & 5G ***(FSC-BW127B only)***	
3	GND	Vss	Power Ground	
4	GND	Vss	Power Ground	
5	GND	Vss	Power Ground	
6	GND	Vss	Power Ground	
7	GND	Vss	Power Ground	
8	GND	Vss	Power Ground	
9	WiFi-2&5G	O	RF I/O port chain0, Wi-Fi 2.4G & 5G	
10	GND	Vss	Power Ground	
11	GND	Vss	Power Ground	

12	BT_ANT	O	RF I/O port chain3, BT 2.4G ***(FSC-BW127B only)***
13	NC		If not used keep NC.
14	NC		If not used keep NC.
15	SD_RESET	I	Reset Pin for SDIO interface, Low for disable SDIO interface ON: pull high; OFF: pull low
16	SD_WAKE	O	WLAN wake-up HOST
17	SDIO_CMD	I/O	SDIO Command Input
18	SDIO_CLK	I	SDIO Clock Input
19	SDIO_D3	I/O	SDIO Data Line 3
20	SDIO_D2	I/O	SDIO Data Line 2
21	SDIO_D0	I/O	SDIO Data Line 0
22	SDIO_D1	I/O	SDIO Data Line 1
23	GND	Vss	Ground
24	NC		If not used keep NC.
25	NC		If not used keep NC.
26	NC		If not used keep NC.
27	NC		If not used keep NC.
28	NC		If not used keep NC.
29	NC		If not used keep NC.
30	NC		If not used keep NC.
31	SUSCLK		External Low Power Clock input (32.768KHz), If not used keep NC.
32	GND	Vss	Power Ground
33	GPIO5	I/O	General Purpose Input/ Output Pin. If not used keep NC.
34	VDD_IO	PWR	I/O Voltage supply input 1.8V or 3.3V (Peak Current:200mA)
35	GPIO4	I/O	General Purpose Input/ Output Pin. If not used keep NC. Do not pull high on this pin.
36	VDD_3V3	PWR	Main power voltage source input 3.3V (Peak Current:1.5A)
37	NC		If not used keep NC.
38	BT_DIS	I	Enable pin for Bluetooth device, External pull low to shutdown BT ON: pull high; OFF: pull low
39	GND	Vss	Power Ground
40	UART _TX	O	Bluetooth UART data out
41	UART _RX	I	Bluetooth UART data in
42	UART _RTS	O	Bluetooth UART RTS
43	UART _CTS	I	Bluetooth UART CTS
44	PCM_CLK	I/O	PCM clock

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45	PCM_SYNC	I/O	PCM sync signal
46	PCM_IN	I	PCM Data input
47	PCM_OUT	O	PCM Data output
48	NC		If not used keep NC.
49	BT_WAKE	I	HOST wake-up BT device
50	UART_WAKE	O	BT device wake-up HOST

4 ELECTRICAL CHARACTERISTICS

4.1 Temperature Limit Ratings

Table 4-1: Temperature Limit Ratings

Parameter	Min	Type	Max	Unit
Temperature Limit Ratings	0		70	°C
Storage Temperature	-40		+85	°C

4.2 DC Characteristic

Table 4-2-1: Power Supply Characteristics

Symbol	Parameter	Min	Type	Max	Peak Current
VDD_3V3	3.3V I/O Supply Voltage	3.0V	3.3V	3.6V	1.5A
VDD_IO	1.8V/3.3V I/O Supply Voltage	1.62V	1.8V/3.3V	3.6V	200mA

Table 4-2-2: Digital IO Pin DC Characteristics -- 3.3V IO

Symbol	Parameter	Min	Type	Max	Units
V_{IH}	Input high voltage	2.0	3.3	3.6	V
V_{IL}	Input low voltage	-	0	0.9	V
V_{OH}	Output high voltage	2.97	-	3.3	V
V_{OL}	Output low voltage	0	-	0.33	V

Table 4-2-3: Digital IO Pin DC Characteristics – 1.8V IO

Symbol	Parameter	Min	Type	Max	Units
V_{IH}	Input high voltage	1.26	1.8	3.6	V
V_{IL}	Input low voltage	-	0	0.8	V
V_{OH}	Output high voltage	1.62	-	1.8	V
V_{OL}	Output low voltage	0	-	0.18	V

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5 PHYSICAL INTERFACE

5.1 SDIO Interface Timing Specification

5.1.1 SDIO Interface AC Characteristics

For timing criteria, please check “SD specifications Part1 Physical Layer Specification Version3.01”

5.1.2 SDIO Interface Signal Levels

The SDIO a signal level ranges from 1.8V to 3.3V.

5.1.3 SDIO Interface Characteristics

For timing criteria, please check specification in “SD specifications Part1 Physical Layer Specification Version 3.01”

5.1.4 Platform state transitions

Table 5-1-4： Power Supply Characteristics

3.3V Power range	3.3V Ripple	3.3V Noise	Rise time Min.	Rise time Max.
+/-0.165V	300mVpp @ switching frequency > 200KHz		0.5ms	5ms

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5.1.5 Power Management Handshake Interface Signal Level

SD_RESET Signal Level

The SD_RESET signal level ranges from 1.8V to 3.3V.

BT_DIS# Signal Level

The BT_DIS# signal level ranges from 1.8V to 3.3V.

5.1.6 System Power on Sequence

3.3V Single Power

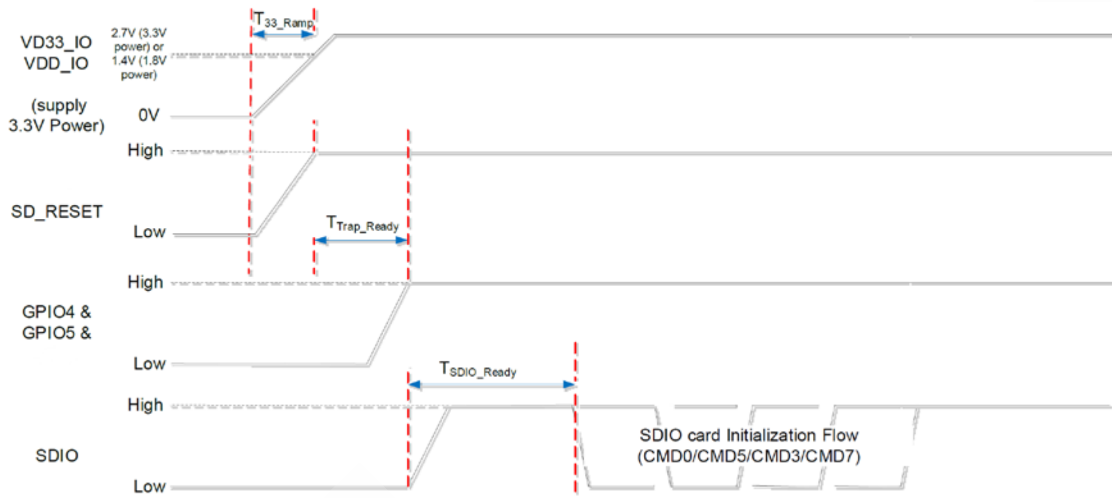

Figure 5-1-6-1: 3.3V Single Power

3.3V and 1.8V Single Power

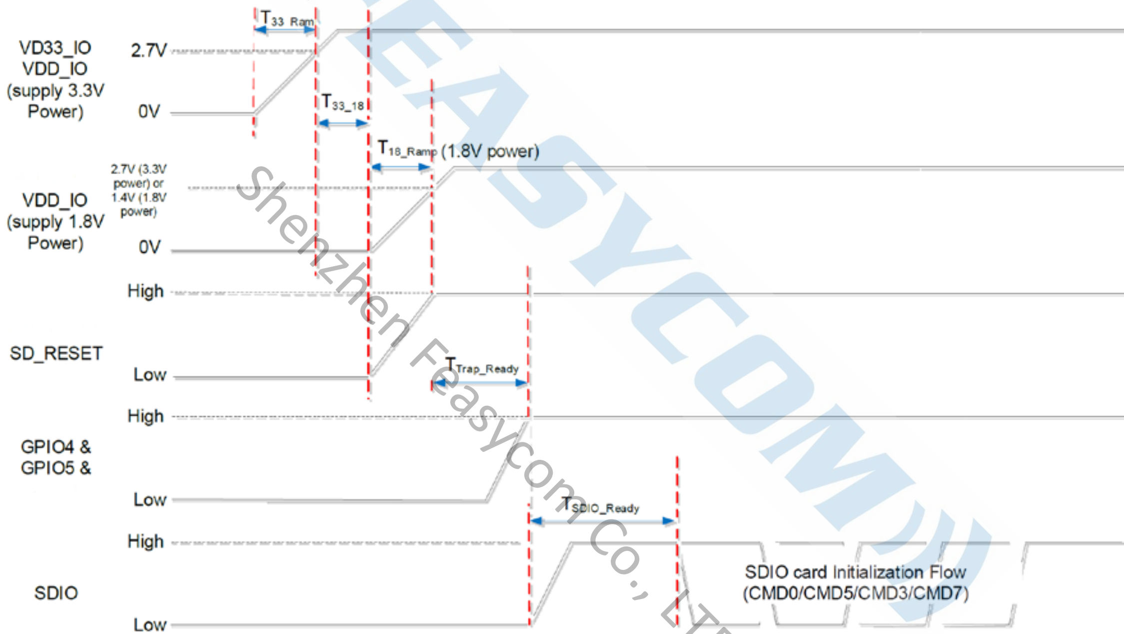

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Figure 5-1-6-2: 3.3V and 1.8V Single Power

Table 5-1-6： System Power on Timing Parameters

	Min.	Typ.	Max.	Unit	Description
T_{18_Ramp}	0.5	1.5	5	ms	The 1.8V power ramp up duration.
T_{33_Ramp}	0.5	1.5	5	ms	The 3.3V power ramp up duration.
T_{33_18}	0	5	x	ms	If 1.8V power is applied, it needs to be equal or slower than 3.3V power.
T_{Trap_Ready}	400	500	x	ms	WLAN eFuse autoload. T_{Trap_Ready} = 500ms (Typical)
T_{SDIO_Ready}	10	20	100	ms	SDIO Not Ready Duration. In this state, the module may respond to commands without the ready bit being set. After the ready bit is set, the host will initiate complete card detection procedure.

➢ **SDIO Interface Power On Sequence**

After power-on, the SDIO interface is selected by the module automatically when a valid SDIO command is received. To attain better SDIO host compatibility, the following power-on sequence is recommended.

We recommend that the card detection procedures are divided into two phases: A 3.3V/1.8V power pre-charge phase and a formal power-up phase.

After the 3.3V ramp up and 1.8V ramp up, the power management unit is enabled by the power ready detection circuit. The power management unit enables the SDIO block. eFUSE is then auto loaded to SDIO circuits during the TSDIO_Ready duration and then SDIO pins are pulled up. After CMD5/5/3/7 procedures, card detection is executed.

➢ **SD_RESET Power On Sequence**

To attain SD_RESET capability, the following power sequence is recommended.

After the 3.3V/1.8V ramp up, the power management unit is enabled by the power ready detection circuit. The power management unit enables the SD_RESET function. After power management unit being enabled, SD_RESET needs to keep high for ensuring WLAN and SDIO function being alive.

5.1.7 WLAN and SDIO Reset Sequence

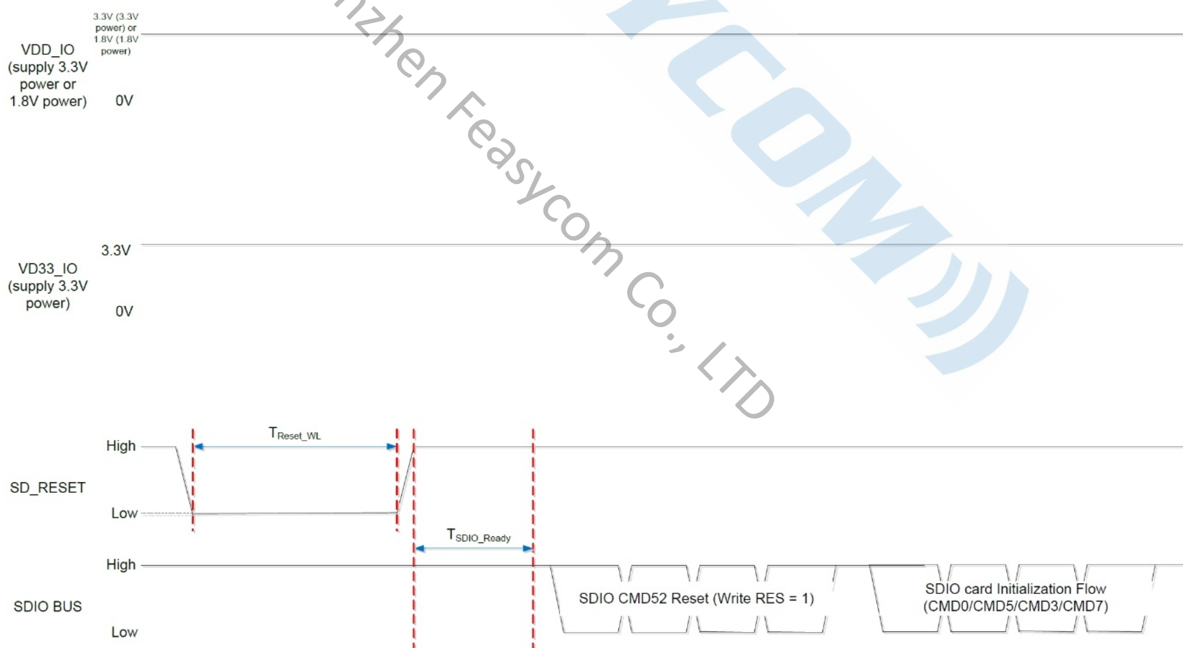

Figure 5-1-7: WLAN and SDIO Reset Sequence

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Table 5-1-7： WLAN and SDIO Reset Timing Parameters

	Min.	Typ.	Max.	Unit	Description
T_{Reset_WL}	100	100	x	ms	SD_RESET keep low duration
T_{SDIO_Ready}	10	20	x	ms	SDIO Not Ready Duration. In this state, the RTL8852BS may respond to commands without the ready bit being set. After the ready bit is set, the host will initiate complete card detection procedure.

5.1.8 SDIO Bus IO Reset Sequence

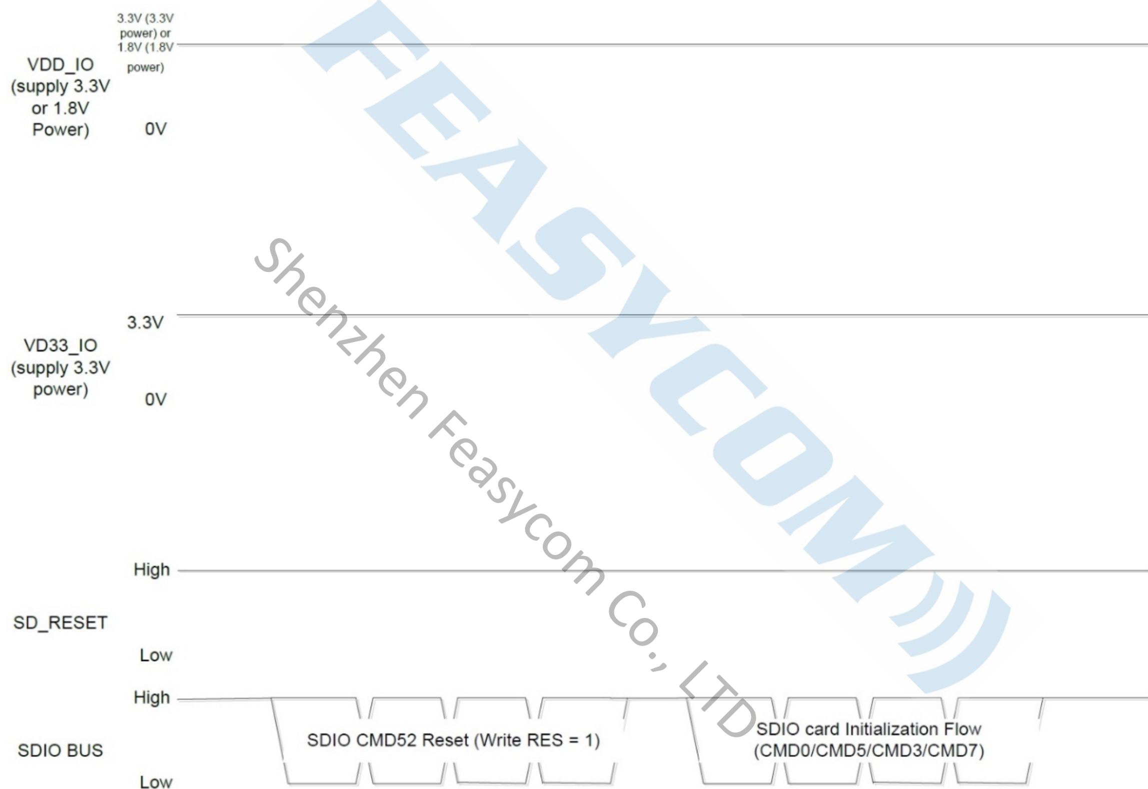

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Figure 5-1-8: SDIO Reset Sequence

5.1.9 System Power off Reset Sequence

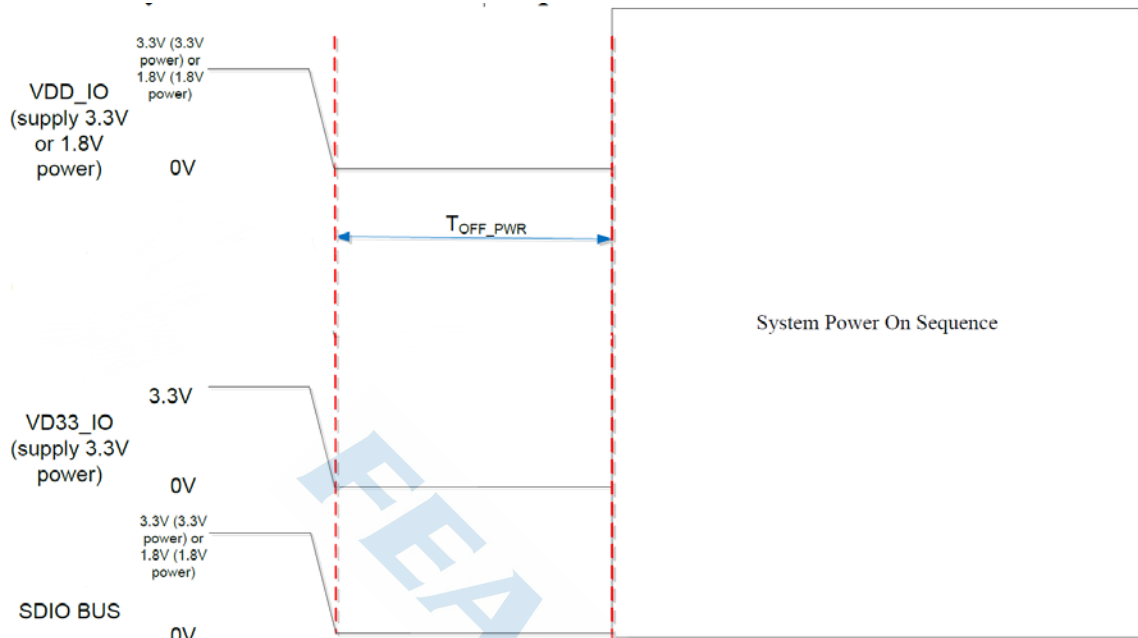

Figure 5-1-9: System Power off Reset Sequence

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The 3.3V/1.8V power should keep low at least T_{OFF_PWR} before calling system power on Sequence.
Main-Power_EN should be pulled high during power reset sequence.

Table 5-1-9： System Power off Reset Timing Parameters

	Min.	Typ.	Max.	Unit	Description
T_{off_PWR}	100	100	x	ms	3.3V/1.8V power keep low duration

5.1.10 BT_DIS Timing Sequence

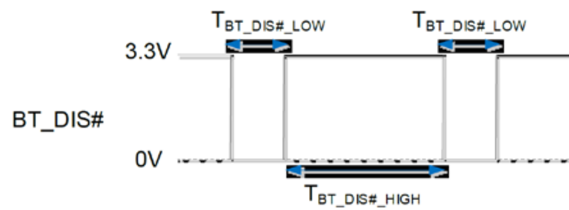

Figure 5-1-10: BT_DIS Timing Sequence

Table 5-1-10： BT_DIS Timing Parameters

	Min.	Typ.	Max.	Unit	Description
BT_DIS#_LOW	200	-	-	ms	BT_DIS# low duration
BT_DIS#_HIGH	200	-	-	ms	BT_DIS# high duration

5.2 UART Interface Characteristics

The UART interface is a 3-wire interface with RX, TX, CTS. The interface supports the Bluetooth 2.0 UART HCI H4 and H5 specifications. The default baud rate is 115.2k baud. In order to support high and low speed baud rate, the FSC-BW127 provides multiple UART clocks.

The UART signal level ranges from 1.8V or 3.3V.

The interface includes four signals, TXD/RXD/CTS. Flow control between the host and the device is byte-wise by hardware. When the UART_CTS signal is set high, the device stops transmitting on the interface. If HCI_CTS is set high in the middle of transmitting a byte, the device finishes transmitting the byte and stops the transmission.

Table 5-2：UART Interface Power-On Timing Parameters

Parameter	Condition	Min.	Typ.	Max.	Unit
Baud Rate error rate	Per byte (including start/stop bit)	-1.3	-	1.3	ms

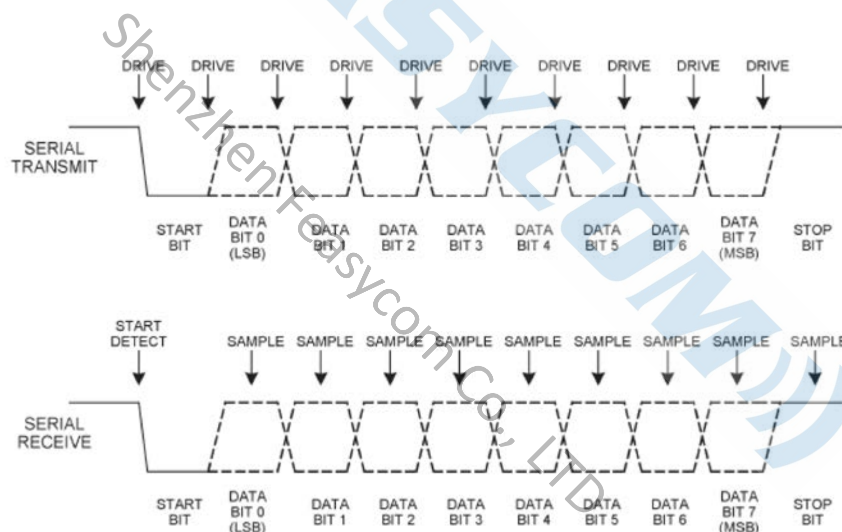

Figure 5-2: UART Interface Waveform

5.2.1 UART Interface Signal Levels

The UART signal level ranges from 1.8V to 3.3V.

5.2.2 UART Interface Timing

The interface includes four signals, TXD/RXD/CTS/RTS. Flow control between the host and the device is byte-wise by hardware. When the UART RX buffer of the device passes the flow-control threshold, the buffer sets the UART_RTS signal high to stop transmission from the host. When the UART_CTS signal is set high, the device stops transmitting on the interface. If HCI_CTS is set high in the middle of transmitting a byte, the device finishes transmitting the byte and stops the transmission.

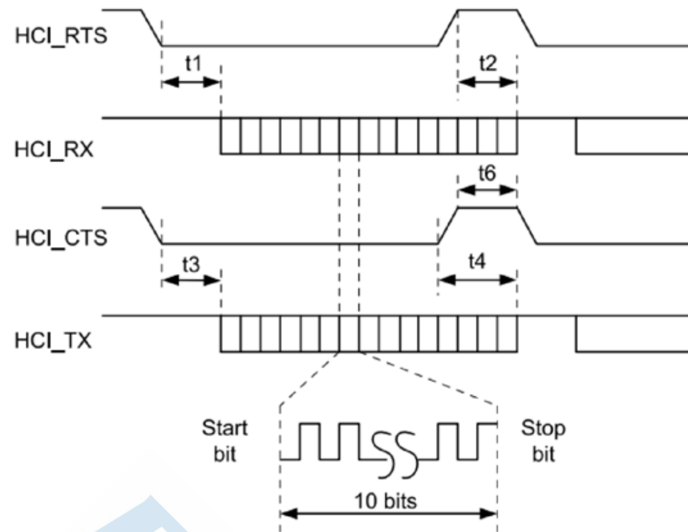

Figure 5-2-2: UART Timing Diagram

Table 5-2-2: UART Interface Power-On Timing Parameters

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
Baud rate			115.2	-	3000	Kbps
Baud rate accuracy per	Receive/Transmit		-3		3	%
CTS low to TX_DATA on		T3	0	2		ns
CTS high to TX_DATA off	Hardware flow	T4			1	byte
CTS High Pulse Width		T6	1			bit
RTS low to RX DATA on		T1	0	2		ns
RST high to RX_DATA off		T2			1	HCI packet*

* Note : HCI packet means HCI command(256 bytes), HCI event(256 bytes), ACL(1024 bytes), SCO(256 bytes)

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5.2.3 UART Interface Power-On Sequence

The UART interface power-on sequence differs depending on whether or not host flow control is supported.

UART Hardware Flow Control Not Supported

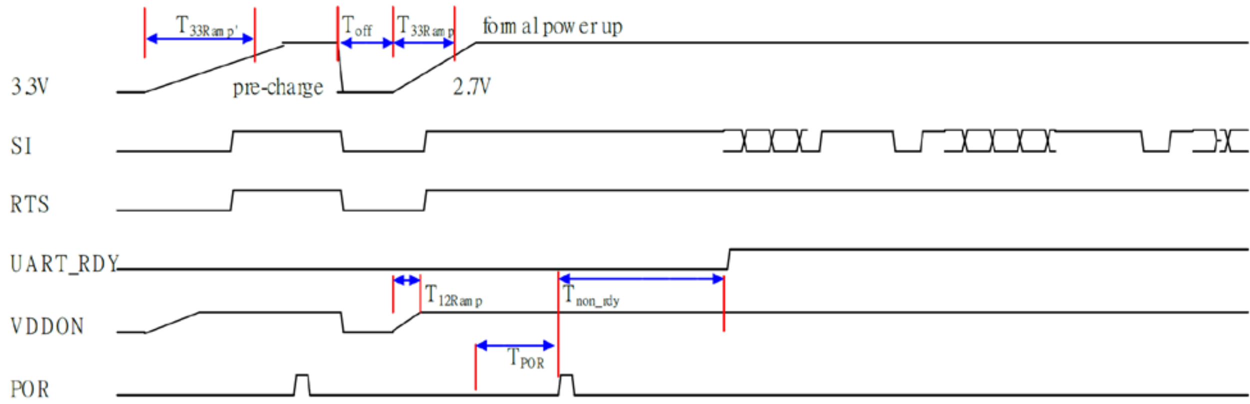

Figure 5-2-3-1: UART Power-On Sequence Without Hardware Flow Control

UART Hardware Flow Control Supported

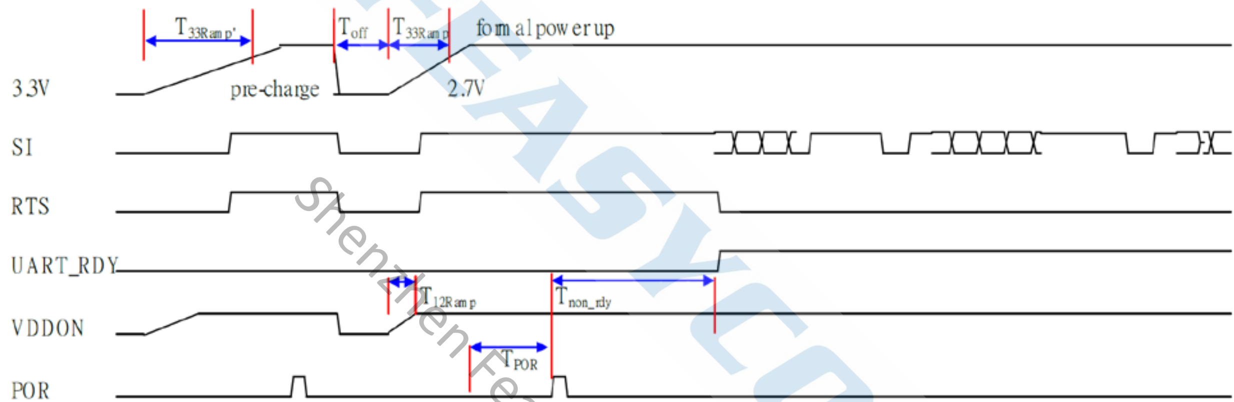

Figure 5-2-3-2: UART Power On Sequence With Hardware Flow Control

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Table 5-2-3-1： UART Interface Power-On Timing Parameters

Symbol	Description
T_{33ramp}	3.3V Power Pre-Charge Ramp Up Duration Before Formal Power Up. We recommend that a 3.3V power-on and then power-off sequence is executed by the host controller before the formal power on sequence. This procedure can eliminate host card detection issues when power ramp up duration is too long, or when a system warm reboot fails.
T_{off}	The duration 3.3V is cut off before formal power up.
T_{33ramp}	The 3.3V main power ramp up duration.
T_{12ramp}	The internal 1.2V ramp up duration.
T_{POR}	The duration from when the power-on reset releases and the power management unit executes power on tasks. A power on reset will detect both 3.3V and 1.2V power ramp up after a predetermined duration.
T_{non_rdy}	UART Not Ready Duration. In this state, the module will not respond to any commands.

We recommend that the card detection procedures are divided into two phases: A 3.3V power pre-charge phase and a formal power-up phase.

During the 3.3V power pre-charge phase, the power ramp up duration is not limited. The 3.3V power is cut off and is turned on after the T_{off} period. The ramp up time is specified in the T_{33ramp} duration.

After main 3.3V ramp up and 1.2V ramp up, the power management unit is enabled by the power ready detection circuit. The power management unit enables the Bluetooth block. The Bluetooth firmware then initializes all circuits included the UART. In addition to wait the T_{non_rdy} time, if the host supports UART hardware flow control it can detect RTS signals and follow the formal UART flow control handshake.

Table 5-2-3-2：UART Interface Power On Timing Parameters

	Min.	Typ.	Max.	Unit
T_{33ramp}	-	-	No Limit	ms
T_{off}	250	500	1000	ms
T_{33ramp}	0.1	0.5	2.5	ms
T_{12ramp}	0.1	0.5	1.5	ms
T_{POR}	2	2	8	ms
T_{non_rdy}	1	2	10	ms

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5.3 PCM Interface Characteristics

The module supports a PCM digital audio interface that is used for transmitting digital audio/voice data to/from the Audio Codec. Features are supported as below:

- Supports Master and Slave mode
- Programmable long/short Frame Sync
- Supports 8-bit A-law/µ-law, and 13/16-bit linear PCM formats
- Supports sign-extension and zero-padding for 8-bit and 13-bit samples
- Supports padding of Audio Gain to 13-bit samples
- PCM Master Clock Output: 64, 128, 256, or 512kHz
- Supports SCO/ESCO link

5.3.1 PCM Format

FrameSync is the synchronizing function used to control the transfer of DAC_Data and ADC_Data. A Long FrameSync indicates the start of ADC_Data at the rising edge of FrameSync (Figure 5-3-1-1), and a Short FrameSync indicates the start of ADC_Data at the falling edge of FrameSync (Figure 5-3-1-2).

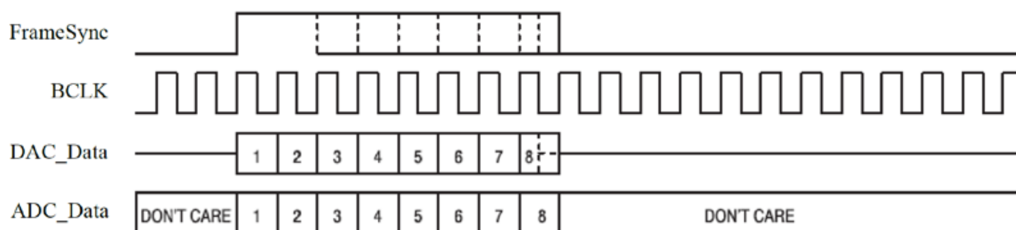

Figure 5-3-1-1: Long FrameSync

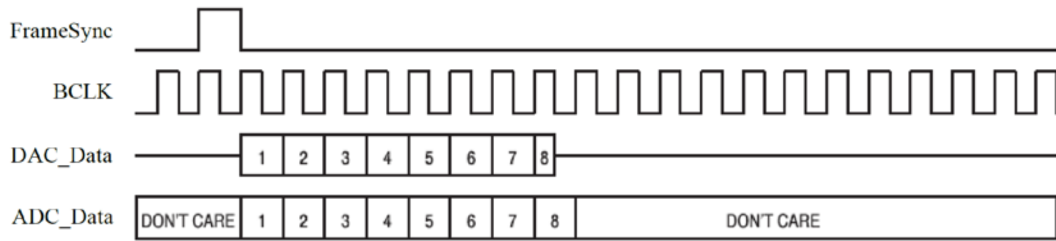

Figure 5-3-1-2: Short FrameSync

5.3.2 Sign Extension and Zero Padding for 8-Bit and 13-Bit Samples

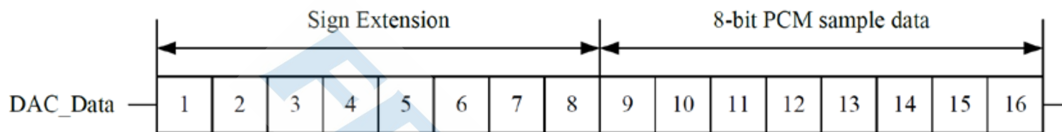

Figure 5-3-2-1: 16-Bit Output Data with 8-Bit PCM Sample Data and Sign Extension

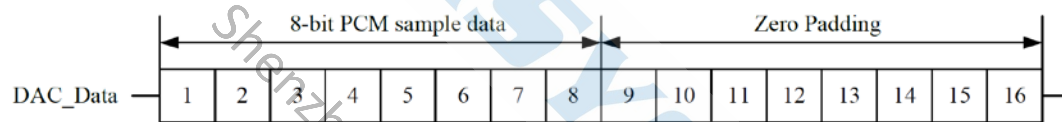

Figure 5-3-2-2: 16-Bit Output Data with 8-Bit PCM Sample Data and Zero Padding

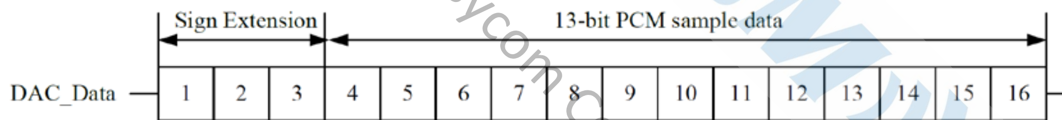

Figure 5-3-2-3: 16-Bit Output Data with 13-Bit PCM Sample Data and Sign Extension

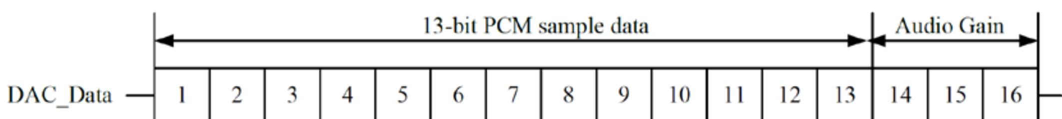

Figure 5-3-2-4: 16-Bit Output Data with 13-Bit PCM Sample Data and Audio Gain

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5.3.3 PCM Interface Timing

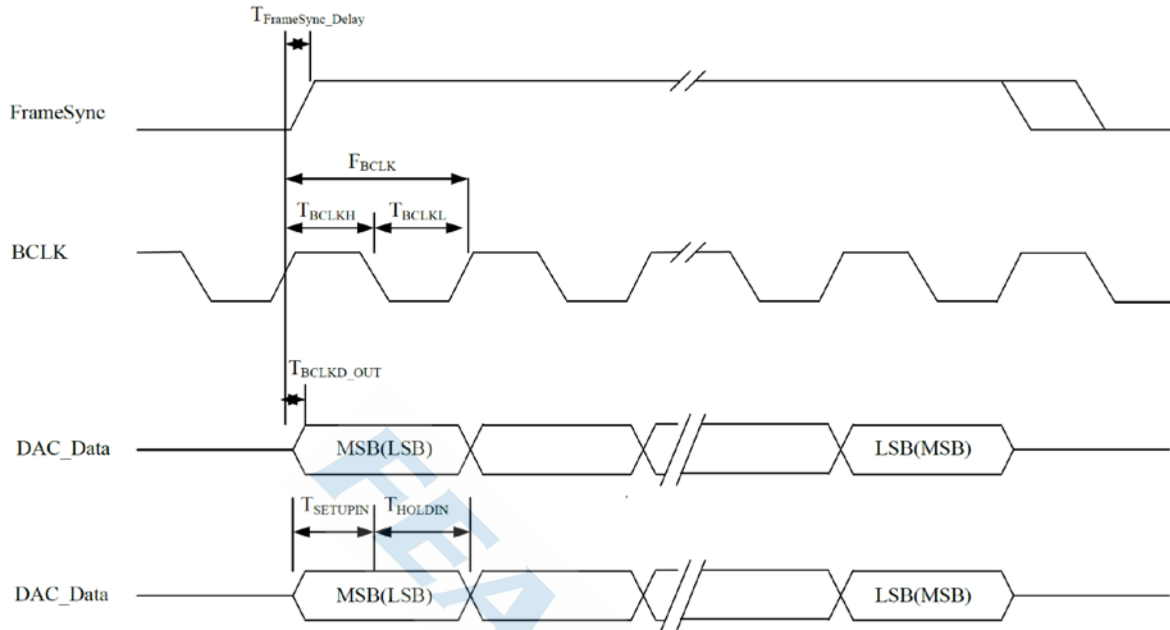

Figure 5-3-3-1: PCM Interface (Long FrameSync)

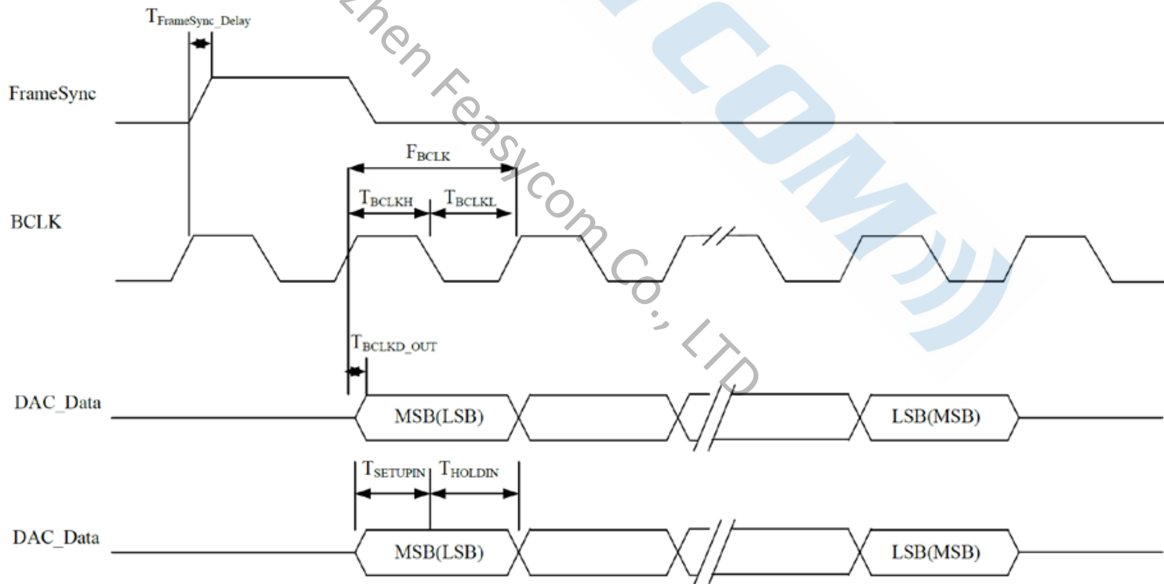

Figure 5-3-3-2: PCM Interface (Short FrameSync)

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Table 5-3-3-1： PCM Interface Clock Specifications

Symbol	Description	Min.	Typ.	Max.	Unit
F_{BCLK}	Frequency of BCLK (Master)	64	-	512	KHz
$F_{FrameSync}$	Frequency of Frame Sync (Master)	-	8	-	KHz
FBCLK	Frequency of BCLK (Slave)	64	-	512	KHz
$F_{FrameSync}$	Frequency of Frame Sync (Slave)	-	8	-	KHz

D	Data Size	8	8	16	bits
N	Number of Slots Per Frame	1	1	1	Slots

Table 5-3-3-2：PCM Interface Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{BCLKH}	High Period of BCLK	980	-	-	ns
T_{BCLKL}	Low Period of BCLK	970	-	-	ns
$T_{FrameSync_Delay}$	Delay Time from BCLK High to Frame Sync High	-	-	75	ns
T_{BCLKD_OUT}	Delay Time from BCLK High to Valid DAC_Data	-	-	125	ns
$T_{SETUPIN}$	Set-up Time for ADC_Data Valid to BCLK Low	10	-	-	ns
T_{HOLDIN}	Hold Time for BCLK Low to ADC_Data Invalid	125	-	-	ns

5.3.4 PCM Interface Signal Levels

The PCM signal level ranges from 1.8V to 3.3V.

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6 MSL & ESD

Table 6-1: MSL and ESD

Parameter	Value
MSL grade:	MSL 3
ESD grade	Electrostatic discharge
ESD – Human Body Model (HBM) Rating JESD22-A114-B	Pass ±2000 V, all pins
ESD – Charged Device Model (CDM) Rating JESD22-C101-D	Pass ±250 V, all pins

7 RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccate (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the below and follow instructions specified by IPC/JEDEC J-STD-033.

Note: The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the below , the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccate and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60%RH.

Notice (注意) :

Feasycom module must use Step-Stencil, suggestion using the stencil thickness about 0.16-0.2mm,it could be modify with the product.

使用我司模块，须使用阶梯钢网，建议阶梯钢网厚度0.16-0.20mm，可根据自己产品适应性，进行相应调整.

Table 7-1: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Feasycom surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

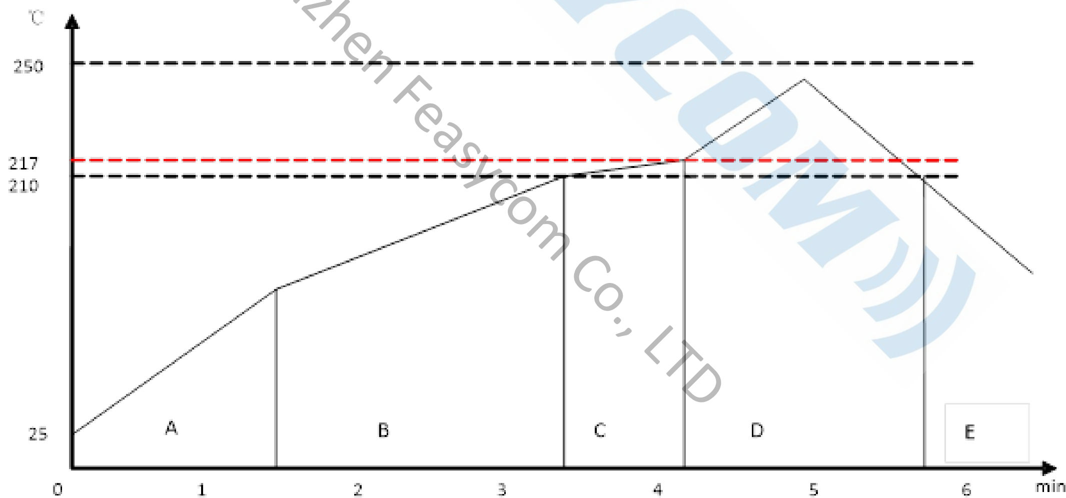

Figure 7-1: Typical Lead-free Re-flow

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Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

Equilibrium Zone 2 (C) (optional) — In order to resolve the upright component issue, it is recommended to

keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

8 MECHANICAL DETAILS

8.1 Mechanical Details

- Dimension: 13mm(W) x 15mm(L) x 2.2mm(H) Tolerance: ±0.2mm
- Module size: 13mm X 15mm Tolerance: ±0.2mm
- Pad size: 1.8mmX0.6mm Tolerance: ±0.1mm
- Pad pitch: 0.9mm Tolerance: ±0.1mm

(分板后边角残留板边误差：不大于 0.5mm) (Residual plate edge error: < 0.5mm)

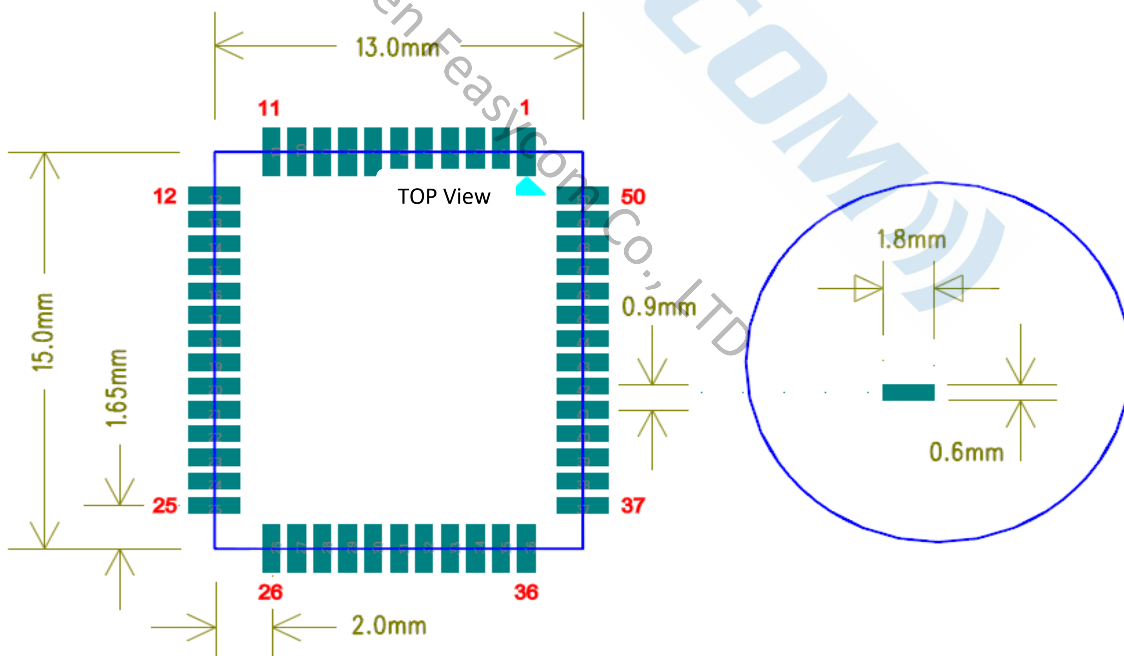

Figure 8-1： FSC-BW127 footprint Layout Guide (Top View)

9 HARDWARE INTEGRATION SUGGESTIONS

9.1 Requirement for the 3.3V power supply

- To use a dedicated power supply circuit for Wi-Fi (and BT).
- <0.05% line regulation and <0.5%/A load regulation are required for ripple frequency below 100KHz.
- Transient-response: 1, The ripple raised from 100/800mA step-response test should be small than 200mVpp.
  2, The ripple swing shall settle down within 1~2 cycles, 2 cycles for the worst case.
- Power supply spur: make sure the spurs from switching mode power supply or other noisy circuits are reasonably small. Once issue concerned with such a power supply spur, alternative power supply filtering might be needed.
- VDD_3V3: 3.0 to 3.6V (Peak Current 1.5A); VDD_IO: 1.7 to 3.6V (Peak Current 200mA)

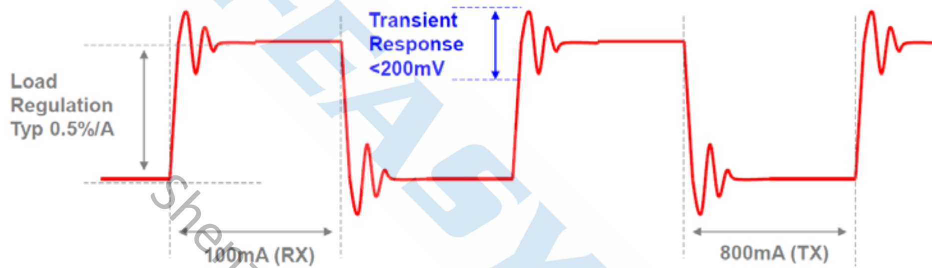

Figure 9-1: Requirement for the 3.3V power supply

9.2 Connections when BT's HCI is by UART

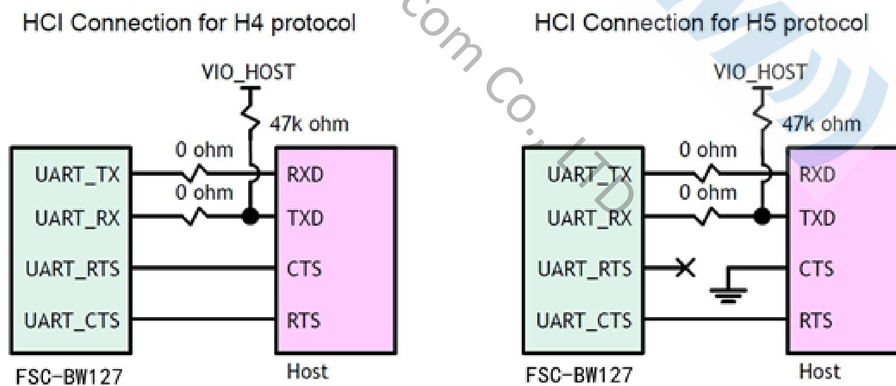

Figure 9-2: Connections when BT's HCI is by UART

Note:

1. Reserve a 47k pull-high resistor on host TXD when this port is not in output mode for default.
   (If not sure, reserve a 47k resistor is recommended for avoid TXD being floating)
2. There must be 0 ohm jumper-resistors on TX/RX paths, for BQB certification test.

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9.3 RF Circuit- RF pads

- Some RF components such as 0402-packaged RLC, connectors, or module pins are with large soldering pad, those pads have higher parasitic capacitance which can impact the characteristic impedance of RF traces.
- The GND under those pads shall be dug out, shown as below, for keeping good 50Ω matching.
- The dig-out layers and area should be calculated carefully, we recommend digging the area a little higher than the simulation results.

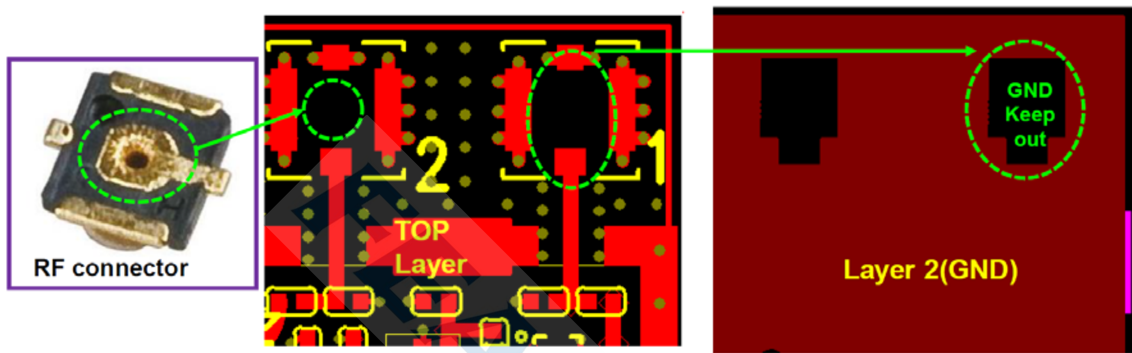

Figure 9-3: RF Circuit- RF pads

9.4 Recommendable antenna & IPEX by Feasycom

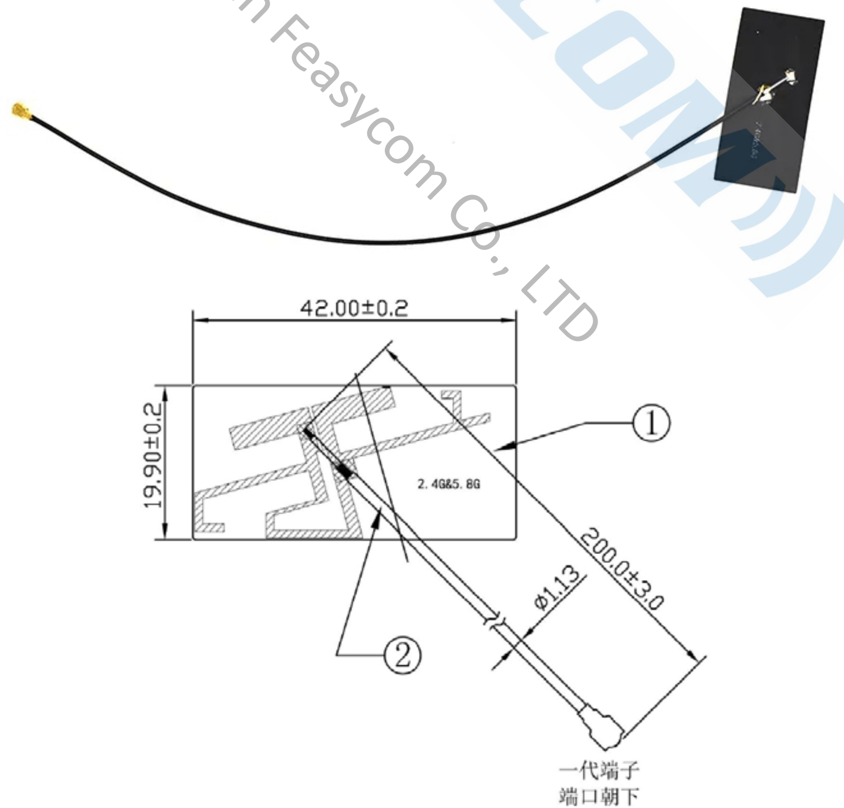

Figure 9-4-1: 2.4GHz & 5GHz Dual-band antenna, with IPEX first generation interface

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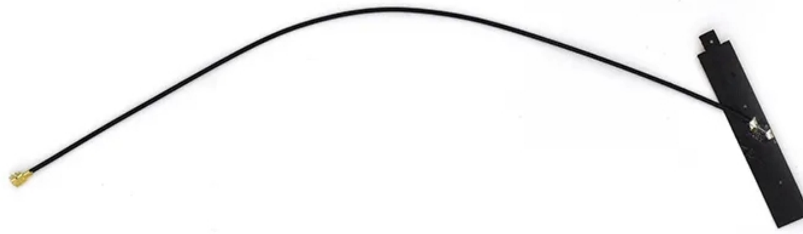

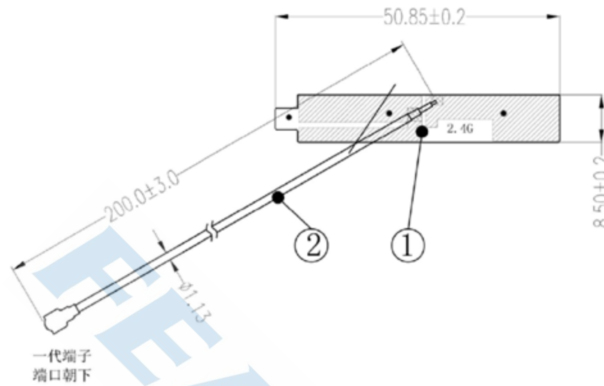

Figure 9-4-2: 2.4GHz antenna with IPEX first generation interface

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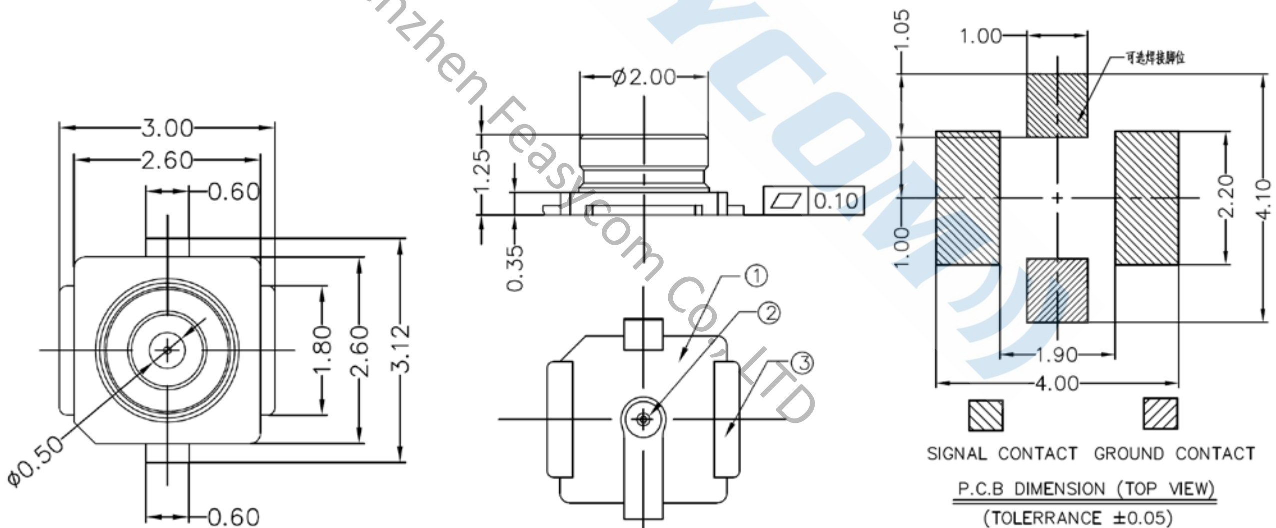

3	GROUND CONTACT	1	JIS C5191-H	Au 1u" Min. over Ni 50~100u" Min.
2	CONTACT	1	JIS C2680-1/4H	Au 1u" Min. over Ni 50~100u" Min.
1	HOUSING	1	LCP E6808	UL94V-0,30% GF
ITEM	NAME	Q'TY	MATERIAL ⚠	FINISH ⚠

NOTES:
1. FREQUENCY RANGE:
   DC TO 6GHZ (VSWR: 1.3MAX AT 0.1~3GHZ, 1.4MAX AT 3~6GHZ)
2. CHARACTERISTIC IMPEDANCE: 50 (NOMINAL);
3. TEMPERATURE: −40°C TO +90°C;
4. RATED VOLTAGE : 60VAC;
5. CONTACT RESISTANCE :
   20m MAX.(SIGNAL CONTACT)
   20m MAX.(GROUND CONTACT)
6. WITHSTAND VOLTAGE : 200VAC FOR 1 MINUTE MIN;
7. INSULATION RESISTANCE : 500M MIN. AT 100VDC;
8. THIS COMPONENT IS HALOGEN FREE.

Figure 9-4-3: IPEX first generation interface

9.5 Soldering Recommendations

FSC-BW127 is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

9.6 Layout Guidelines (Internal Antenna)

Important Note: The antenna for FSC-BW127 is suggested to support both 2.4GHz and 5.8GHz dual frequency bands. We recommend using external FPC dual-band antennas instead of PCB onboard antennas. The following are general instructions for PCB onboard antennas for reference only.

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.

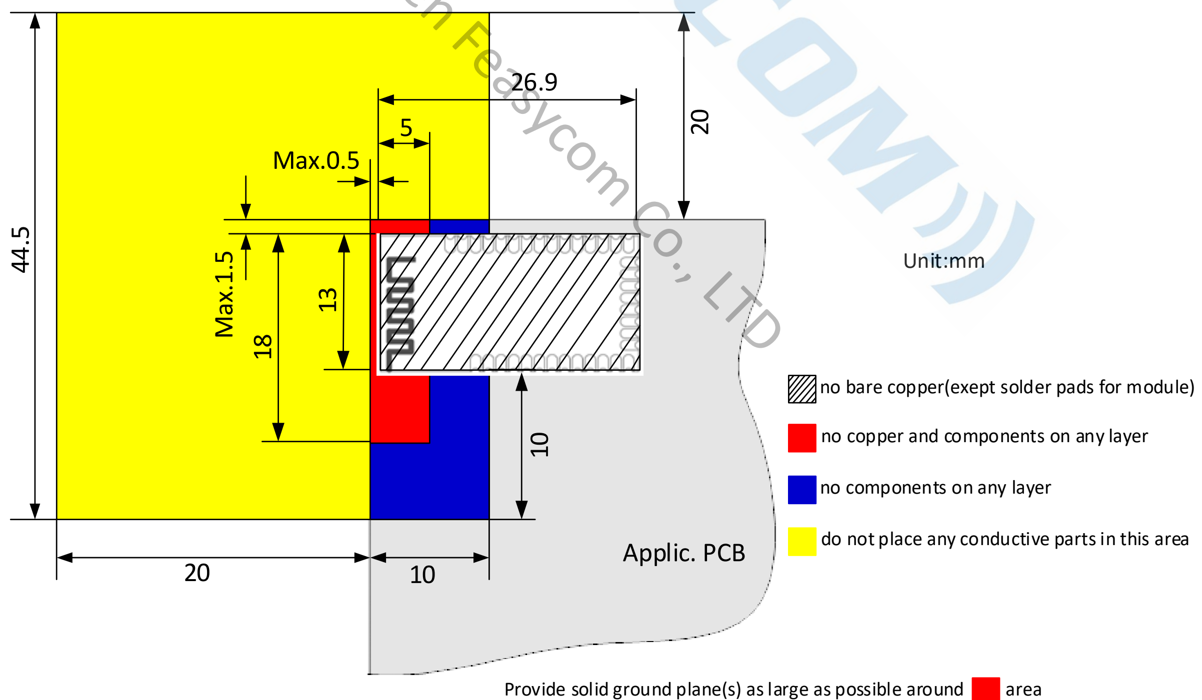

Figure 9-6: Restricted Area (Design schematic, for reference only. Unit: mm)

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid

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problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

9.7 Layout Guidelines(External Antenna)

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

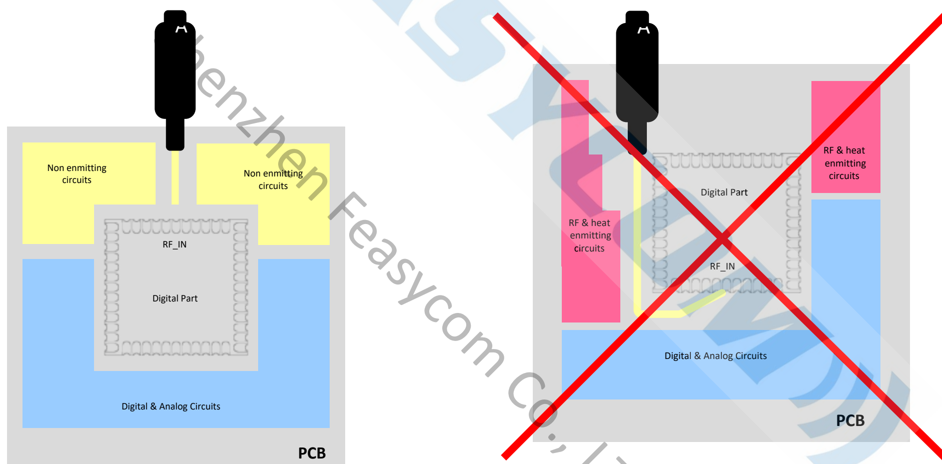

Figure 9-7: Placement the Module on a System Board

9.7.1 Antenna Connection and Grounding Plane Design

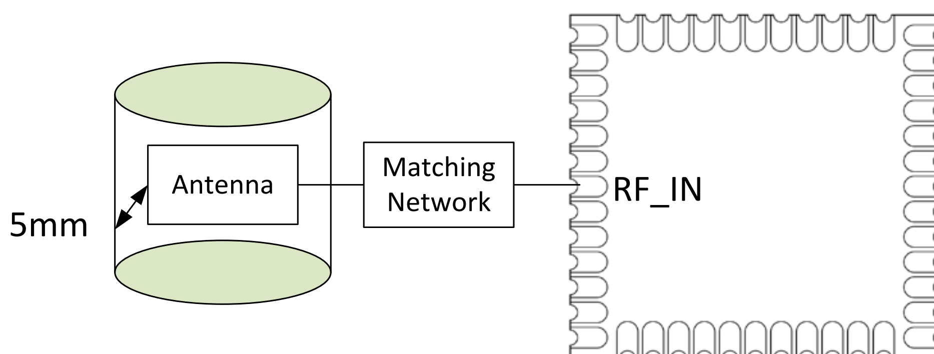

Figure 9-6-1: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

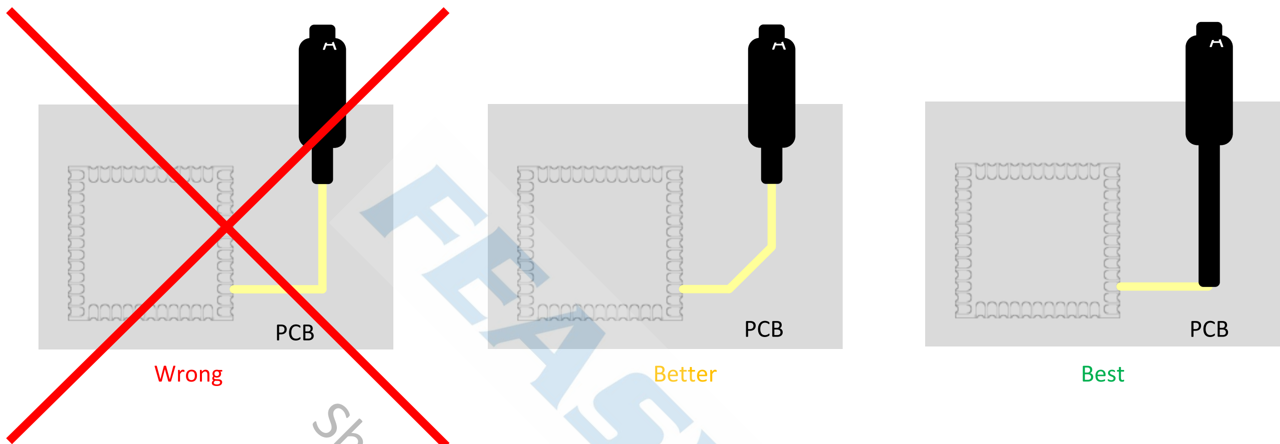

Figure 9-6-2: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

9.8 SDIO Lines Layout Guideline

The following SDIO line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive 8mA.

SDIO_CMD

SDIO_CLK

SDIO_D0 ~ SDIO_D3

The route length of these signals be less than 15 cm and the line impedance be less than 50Ω

9.9 HCI Lines Layout Guideline

The following HCI line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive 4 ~ 8mA

UART_RX

UART_TX

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UART_CTS

UART_RTS

The route length of these signals be less than 15cm and the line impedance be less than 50Ω

9.10 Power Trace Lines Layout Guideline

VDD_3V3 Trace Width: 40mil

VDD_IO Trace Width: 20mil

9.11 Ground Lines Layout Guideline

A Complete Ground in Ground Layer.

Add Ground Through Holes to FSC-BW127 Module Ground Pads

Decoupling Capacitors close to FSC-BW127 Module Power and Ground Pads

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10 PRODUCT PACKAGING INFORMATION

10.1 Default Packing

a, Tray vacuum

b, Tray Dimension: 240mm * 185mm

Figure 10-1: Tray vacuum

10.2 Packing box (Optional)

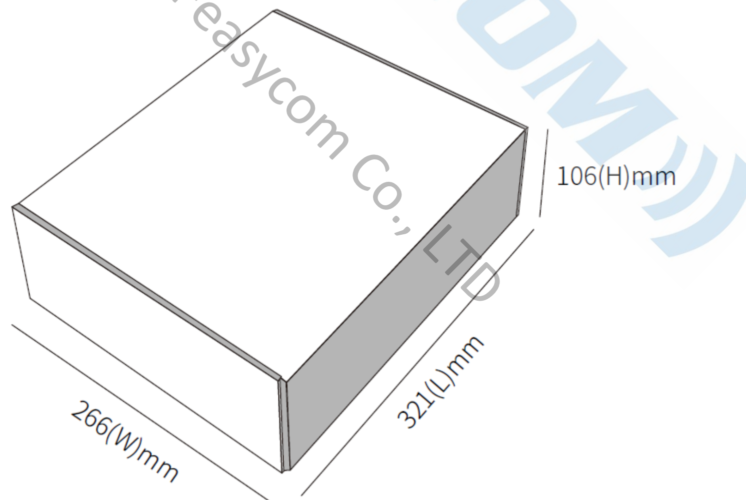

Figure 10-2: Packing box(Optional)

** If other packing is required, please confirm with the customer*

** Packing: 1000pcs per carton (Minimum packing quantity)*

** The outer packing size is for reference only, please refer to the actual size*

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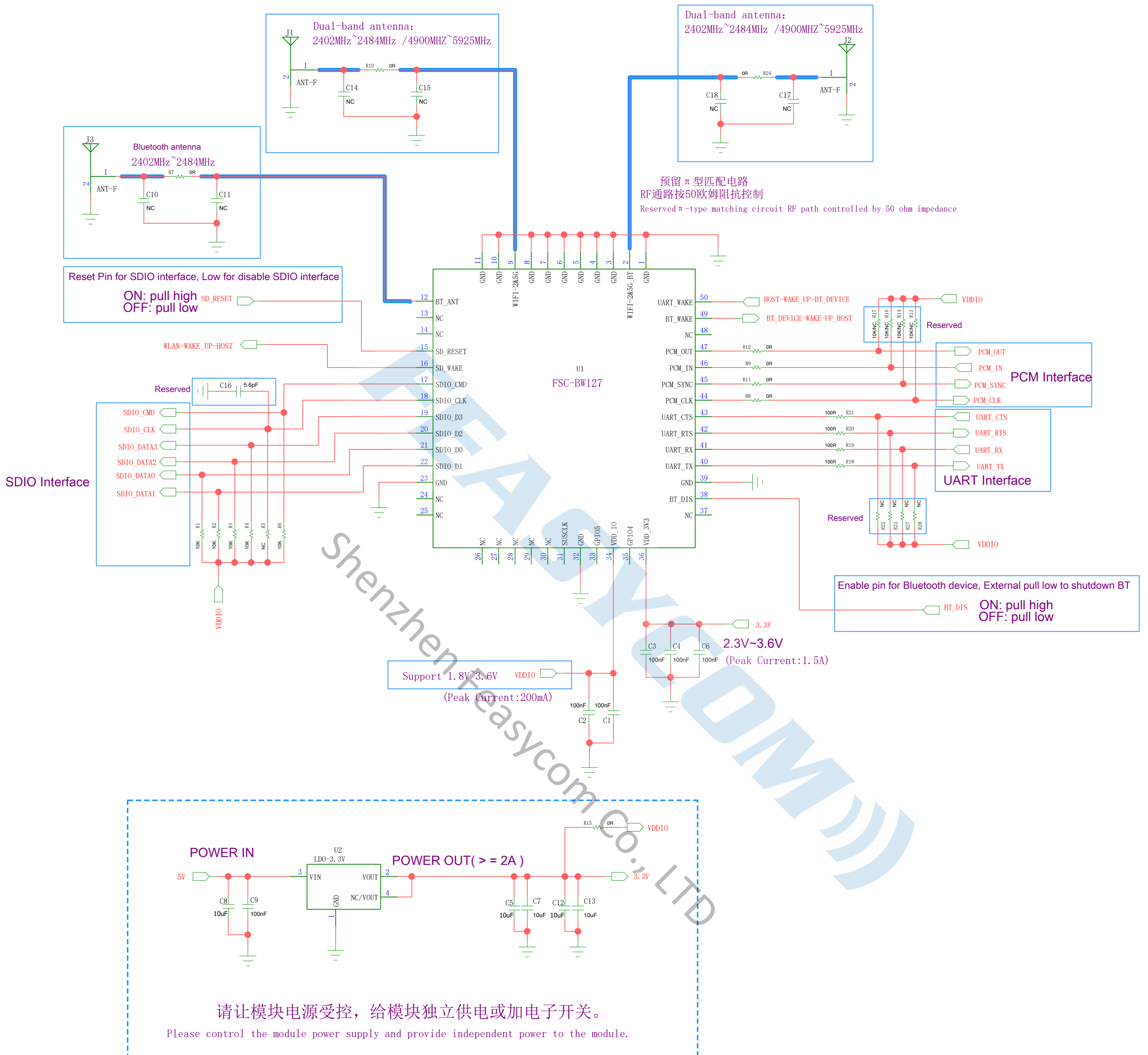
11 APPLICATION SCHEMATIC



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