FSC-BW110

Wi-Fi Single-band 1X1 + Bluetooth 2.1+ EDR/Bluetooth 3.0/3.0 + HS/4.2 Combo Module Datasheet

Version 1.1

Revision History

Version	Data	Notes	
1.0	2021/04/23	Initial Version	Fish
1.1	2021/04/27	Optimize pictures	Fish

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Contents

1. INTRODUCTION

Overview

FSC-BW110 is a small size and low profile of Wi-Fi + BT Combo module with LGA(Land-Grid Array) footprint, board size is 12mm*12mm with module thickness of 1.9mm. It can be easily manufactured on SMT process and highly suitable for tablet PC, ultra book, mobile device and consumer products. It provides SDIO interface for Wi-Fi to connect with host processor and high speed UART interface for BT. It also has a PCM interface for audio data transmission with direct link to external audio codec via BT controller. The Wi-Fi throughput can go up to 150Mbps in theory by using 1x1 802.11n b/g/n MIMO technology and Bluetooth can support BT2.1+EDR/BT3.0 and BT4.2. FSC-BW110 uses highly integrated Wi-Fi/BT single chip based on advanced COMS process. FSC-BW110 integrates whole Wi-Fi/BT function blocks into a chip, such as SDIO/UART, MAC, BB, AFE, RFE, PA, EEPROM and LDO/SWR, except fewer passive components remained on PCB.

This compact module is a total solution for a combination of Wi-Fi + BT technologies. The module is specifically developed for Smart phones and Portable devices.

Features

- Operate at ISM frequency bands (2.4GHz)
- SDIO for Wi-Fi and UART for Bluetooth
- IEEE standards support: IEEE 802.11b, IEEE 802.11g, IEEE 802.11n, IEEE 802.11d, IEEE 802.11e, IEEE 802.11h, IEEE 802.11i
- Fully Qualified for Bluetooth 2.1+EDR specification including both 2Mbps and 3Mbps modulation mode
- Fully qualified for Bluetooth 3.0
- Fully qualified for Bluetooth 4.2 Dual mode
- Full–speed Bluetooth operation with Piconet and Scatternet support
- Enterprise level security which can apply WPA/WPA2 certification for Wi-Fi.
- Wi-Fi 1 transmitter and 1 receiver allow data rates supporting up to 150 Mbps downstream and 150 Mbps upstream PHY rates

2. General Specification

Table 1: General Specifications

Categories	Implementation
Model Name	BW110
Product Description	Support Wi-Fi/Bluetooth functionalities
Dimension	L x W x H: 12 x 12 x1.8 (typical) mm
Wi-Fi Interface	Support SDIO V2.0
BT Interface	UART / PCM
Operating temperature	0°C to 70°C
Storage temperature	-40°C to 85°C
RoHS	All hardware components are fully compliant with EU RoHS directive

3. Recommended Operating Rating

The digital IO supports VDD33 or VDD18 application.

Table 2: Recommended Operating Rating

Parameter	Min	Type	Max	Unit
Operating Temperature	0	25	70	°C
VCC33	3.15	3.3	3.45	V
VDDIO	1.7	1.8 or 3.3	3.45	V

4. Wi-Fi/BT RF Specification

4.1 2.4GHz RF Specification

Table 3: 2.4GHz RF specification

Feature	Description			
Operating Frequency	2.400～2.4835GHz			
Spectrum Mask	**Min. b/g/n**	**Typ. b/g/n**	**Max. b/g/n**	**Unit b/g/n**
1st side lobes(to fc ± 11MHZ)		-42/-38/-32		dBr
2st side lobes(to fc ± 22MHZ)		-52/-60/-60		dBr
Freq. Tolerance	-20/-20/-20		20/20/20	ppm
Standards	Wi-Fi: IEEE 802.11b, IEEE 802.11g, IEEE 802.11n, IEEE 802.11d, IEEE 802.11e, IEEE 802.11h, IEEE 802.11i BT: V2.1+EDR/BT v3.0/BT v3.0+HS/BT v4.2			
Modulation	Wi-Fi: 802.11b: CCK(11, 5.5Mbps), QPSK(2Mbps),			

	BPSK(1Mbps), 802.11 g/n: OFDM BT: 8DPSK, π/4 DQPSK, GFSK
PHY Data rates	Wi-Fi: 802.11b: 11,5.5,2,1 Mbps 802.11g: 54,48,36,24,18,12,9,6 Mbps 802.11n: up to 150Mbps BT: 1 Mbps for Basic Rate 2,3 Mbps for Enhanced Data Rate
Transmit Output Power	Wi-Fi: 802.11b@11 Mbps 17±1.5dBm 802.11g@54 Mbps 14±1.5dBm 802.11n@65 Mbps 13±1.5dBm(MCS 7_HT20) 13±1.5dBm(MCS 7_HT40) BT: Max +10dBm
EVM	802.11b /1Mbps : EVM≦-10dB 802.11b /11Mbps : EVM≦-10dB 802.11g /6Mbps : EVM≦-5dB 802.11g /54Mbps : EVM≦-25dB 802.11n/6.5Mbps : EVM≦-5dB 802.11n/65Mbps : EVM≦-28dB 802.11n/13.5Mbps : EVM≦-5dB 802.11n/135Mbps : EVM≦-28dB
Receiver Sensitivity (Wi-Fi)	802.11b@8% PER 1Mbps ≦-91dBm 2Mbps≦ -89dBm 5.5Mbps≦ -87dBm 11Mbps ≦-85dBm Max input level≥-8
	802.11g@10% PER 6Mbps ≦-87dBm 9Mbps ≦-86dBm 12Mbps≦ -84dBm 18Mbps≦ -82dBm 24Mbps≦ -79dBm 36Mbps≦ -75dBm 48Mbps ≦-71dBm 54Mbps ≦-70dBm Max input level≥-20
	802.11n@10% PER HT20_MCS 0 ≦-87dBm HT40_MCS 0≦-84 HT20_MCS 1≦ -84dBm HT40_MCS 1≦-81 HT20_MCS 2 ≦-82dBm HT40_MCS 2≦-79 HT20_MCS 3 ≦-79dBm HT40_MCS 3≦-76

	HT20_MCS 4 ≦-75dBm HT40_MCS 4≦-72 HT20_MCS 5 ≦-71dBm HT40_MCS 5≦-68 HT20_MCS 6 ≦-70dBm HT40_MCS 6≦-67 HT20_MCS 7 ≦-69dBm HT40_MCS 7≦-66 Max input level≥-20
Receiver Sensitivity (BT)	-89dBm @ 1Mbps -86dBm @ 2Mbps -83dBm @ 3Mbps
Operating Channel	Wi-Fi 2.4GHz: 11: (Ch. 1-11) – United States 13: (Ch. 1-13) – Europe 14: (Ch. 1-14) – Japan BT 2.4GHz: Ch. 0 ~78
Media Access Control	Wi-Fi: CSMA/CA with ACK BT: AFH, Time Division
Antenna	External Antenna
Network Architecture	Wi-Fi: Ad-hoc mode (Peer-to-Peer) Infrastructure mode Software AP Wi-Fi Direct BT: Pico Net, Scatter Net
Security	Wi-Fi: WPA, WPA-PSK, WPA2, WPA2-PSK, WEP 64bit & 128bit, IEEE 802.11x, IEEE 802.11i BT: Simple Paring
OS Supported	Android /Linux
Host Interface	Wi-Fi: SDIO BT: UART
Operating Voltage	3.3±10% Vdc I/O supply voltage
Dimension	Typical L12.0*W12.0*H1.8mm

5. Power Consumption

Table 4: Power Consumption

Categories	Implementation
Power Consumption (Typical by using SWR)	Wi-Fi only: TX n mode 40MHz: 133 mA RX n mode 40MHz: 53 mA TX n mode 20MHz: 137 mA RX n mode 20MHz: 47 mA

6. Pin Assignments

6.1 PIN Outline

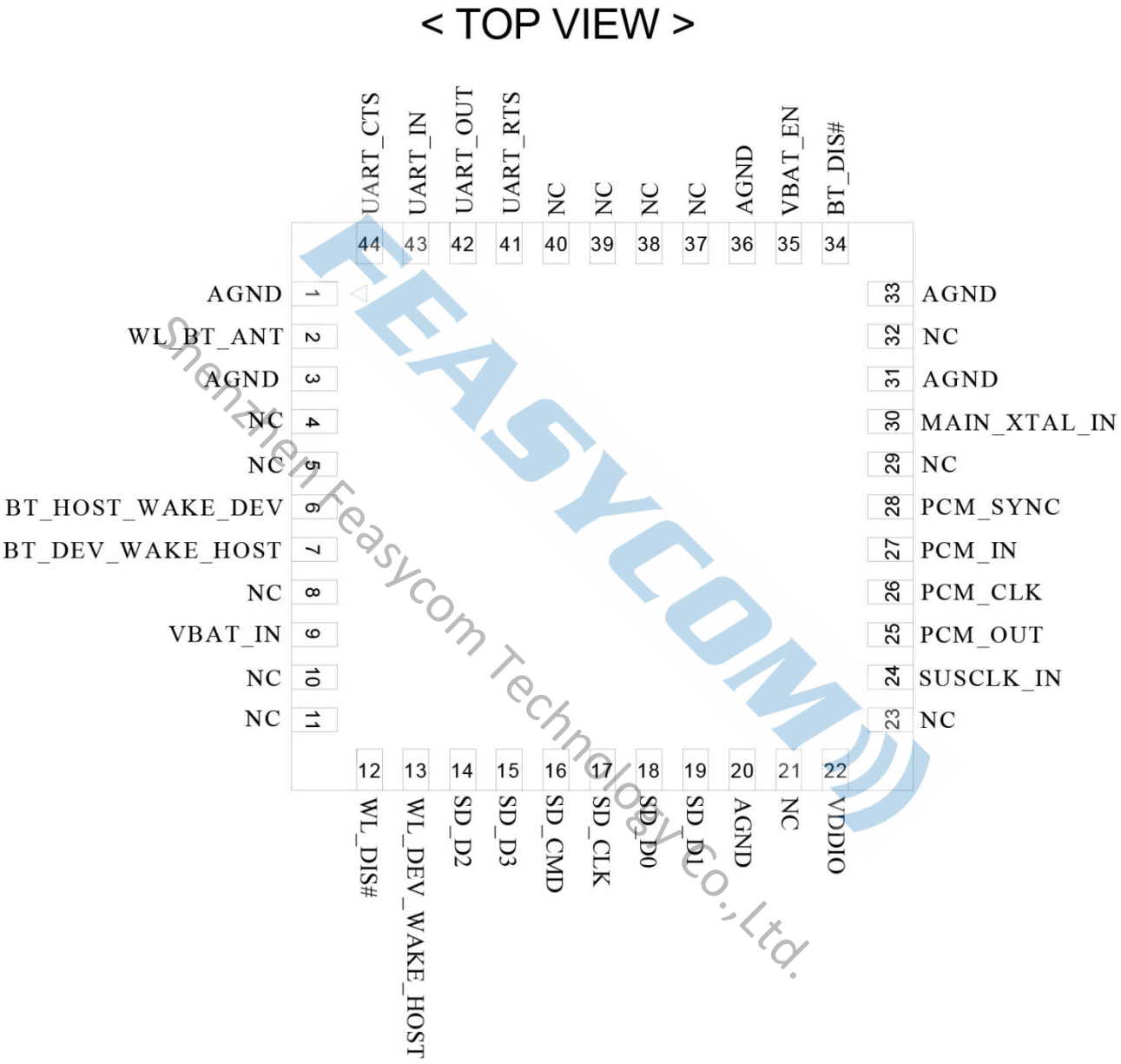


Figure 1: FSC-BW110 PIN Diagram(Top View)

6.2 PIN Definition Descriptions

Table 5: Pin definition

Pin	Pin Name	Type	Pin Descriptions	Voltage
1	AGND		Ground connections	
2	WL_BT_ANT	I/O	RF I/O port	

3	AGND		Ground connections	
4	NC		Floating (NC)	
5	NC		Floating (NC)	
6	HOST_WAKE_BT	I	Host to wake up Bluetooth device	VDDIO
7	BT_WAKE_HOST	O	Bluetooth device to wake up host	VDDIO
8	NC		Floating (NC)	
9	VBAT_IN	P	3.3±10% V Main power voltage source input	3.3V
10	NC		Floating (NC)	
11	NC		Floating (NC)	
12	WL_DIS#	I	Pull high: ON , Pull low: OFF External pull low can disable WL	3.3V
13	WL_HOST_WAKE	O	WLAN to wake up HOST	VDDIO
14	SD_D2	I/O	SDIO data line 2	
15	SD_D3	I/O	SDIO data line 3	
16	SD_CMD	I/O	SDIO command line	
17	SD_CLK	I	SDIO clock line	
18	SD_D0	I/O	SDIO data line 0	
19	SD_D1	I/O	SDIO data line 1	
20	AGND		Ground connections	
21	NC		Floating(NC)	
22	VDDIO	P	I/O Voltage supply input	3.3V
23	NC		Floating (NC)	
24	SUSCLK_IN	I	External Clock input(32.768kHz), or UART_CTS. need to be reserved	
25	PCM_OUT	O	PCM Output	VDDIO
26	PCM_CLK	I/O	PCM Clock	VDDIO
27	PCM_IN	I	PCM Input	VDDIO
28	PCM_SYNC	O	PCM Sync	VDDIO
29	NC		Floating (NC)	
30	MAIN_XTAL_IN	O	Floating (NC)	
31	AGND		Ground connections	
32	NC		Floating (NC)	
33	AGND		Ground connections	
34	BT_DIS#	I	Pull high: ON , Pull low: OFF External pull low can disable BT	3.3V
35	VBAT_EN	P	Floating	
36	AGND		Ground connections	
37	NC		Floating (NC)	
38	NC		Floating (NC)	
39	NC		Floating (NC)	
40	NC		Floating (NC)	
41	UART_RTS		UART CTS module side is Ground connections	
42	UART_OUT	O	UART Output	VDDIO
43	UART_IN	I	UART Input	VDDIO

44	UART_CTS	I	UART CTS	VDDIO

P:POWER I:INPUT O:OUTPUT VDDIO:3.3V

7. Host Interface Timing Diagram

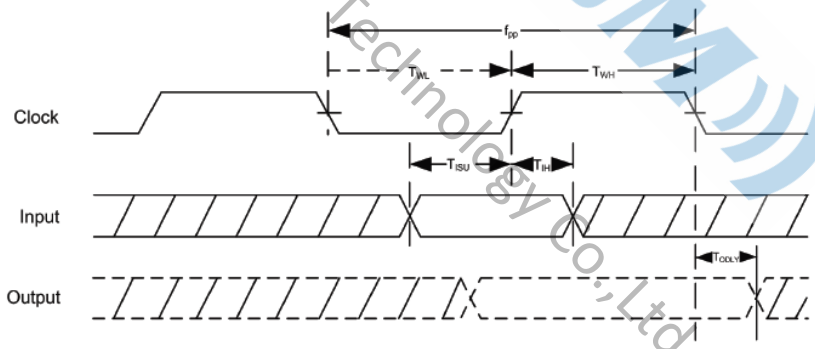
7.1 SDIO Pin Description

The module supports SDIO version 3.0 for all 1.8V 4-bit UHSI speeds: SDR12 (25 Mbps), and SDR25(50Mbps) in addition to the 3.3V default speed(25MHz) and high speed (50MHz). It has the ability to stop the SDIO clock and map the interrupt signal into a GPIO pin. This ‘out-of-band’ interrupt signal notifies the host when the WLAN device wants to tum on the SDIO interface. The ability to force the control of the gated clocks from within the WLAN chip is also provided.

Table 6: SDIO Pin Description

SD 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1 or Interrupt
DATA2	Data Line 2 or Read Wait
DATA3	Data Line 3
CLK	Clock
CMD	Command Line

7.2 SDIO Default Mode Timing Diagram

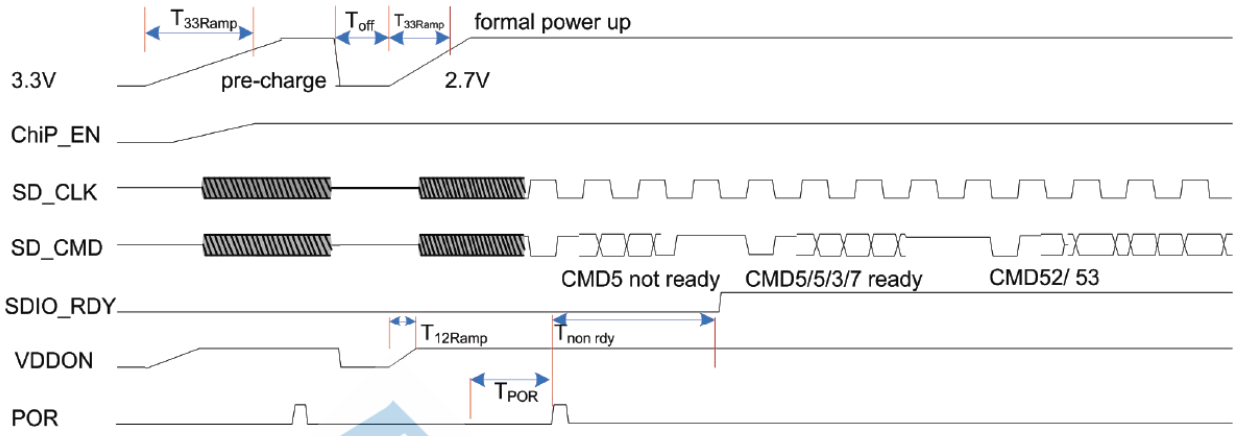


SDIO Interface Timing

SDIO Interface Timing Parameters

NO	Parameter	Mode	MIN	MAX	Unit
f_{pp}	Clock Frequency	Default	0	25	MHz
		HS	0	50	MHz
T_{WL}	Clock Low Time	DEF	10	-	ns
		HS	7	-	ns
T_{WH}	Clock High Time	DEF	10	-	ns
		HS	7	-	ns
T_{ISU}	Input Setup Time	DEF	5	-	ns
		HS	6	-	ns
T_{IH}	Input Hold Time	DEF	5	-	ns
		HS	2	-	ns
T_{ODLY}	Output Delay Time	DEF	-	14	ns
		HS	-	14	ns

7.3 SDIO Power-on sequence



Symbol	Min	Typical	Max	Unit
T_{33ramp}	0.2	-	No Limit	ms
T_{off}	250	500	1000	ms
T_{33ramp}	0.2	0.5	2.5	ms
T_{12ramp}	0.1	0.5	1.5	ms
T_{POR}	2	2	8	ms
T_{non_rdy}	1	2	10	ms

8. RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccate (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the below and follow instructions specified by IPC/JEDEC J-STD-033.

Note: The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the below , the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccate and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60%RH.

Table 6: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven

temperatures during reflow meet the requirements of the solder paste. Feasycom surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

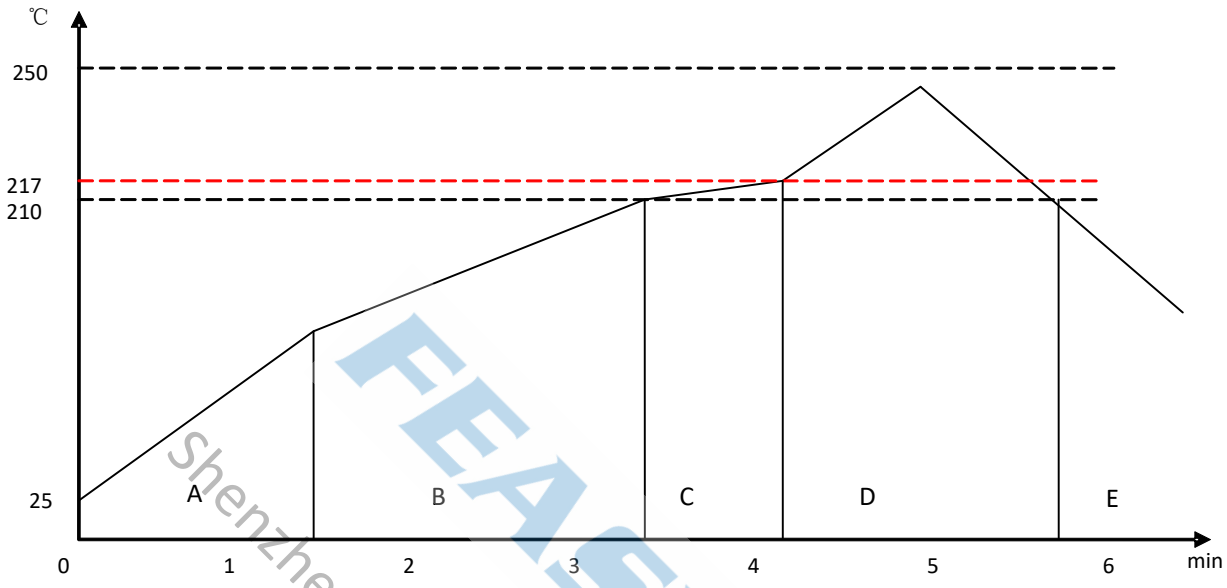


Figure 2: Typical Lead-free Re-flow

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

Equilibrium Zone 2 (C) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

9. MECHANICAL DETAILS

9.1 Physical Dimensions

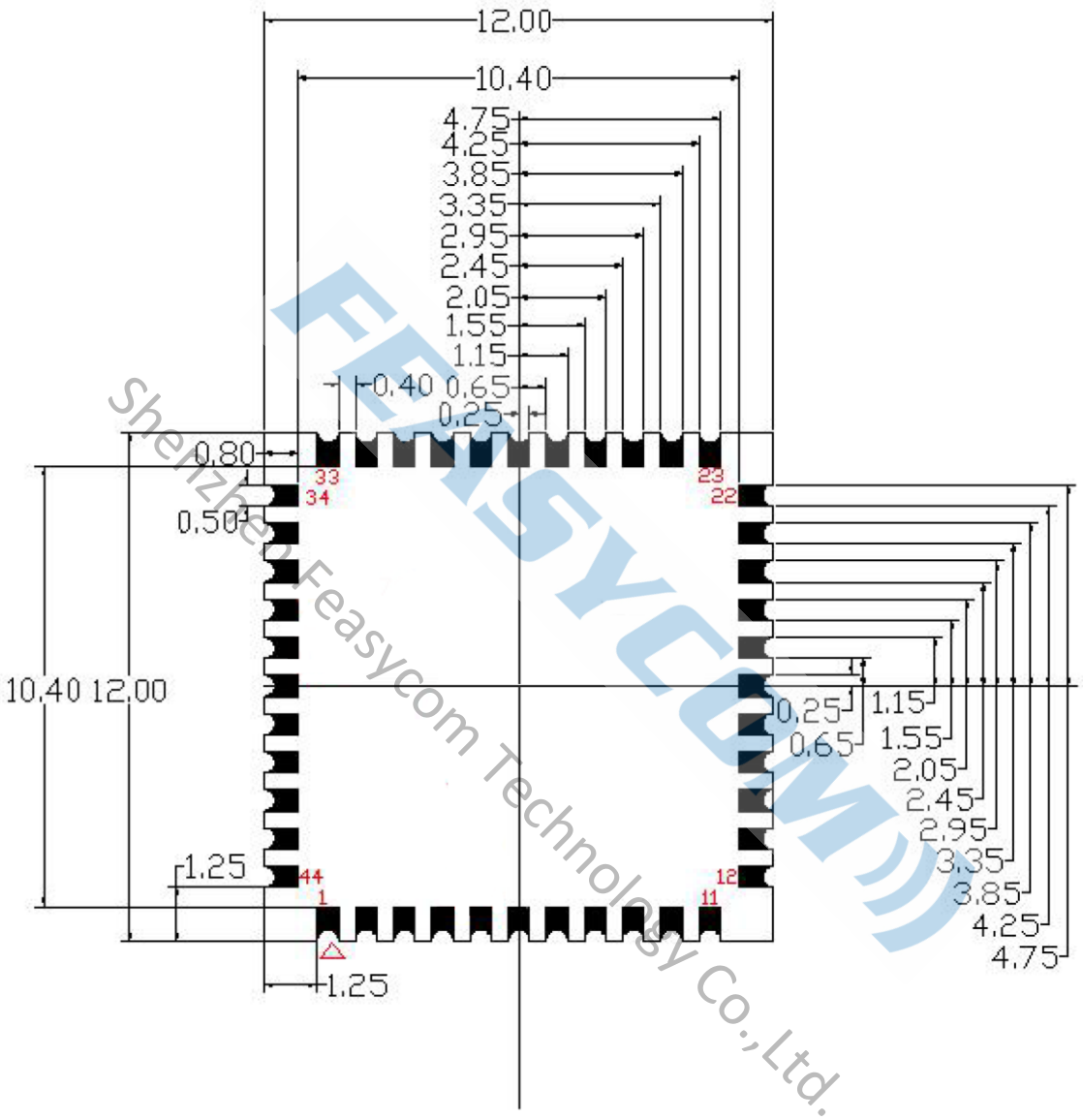


Figure 3: FSC-BW110 Physical Dimensions

9.2 Layout Recommendation

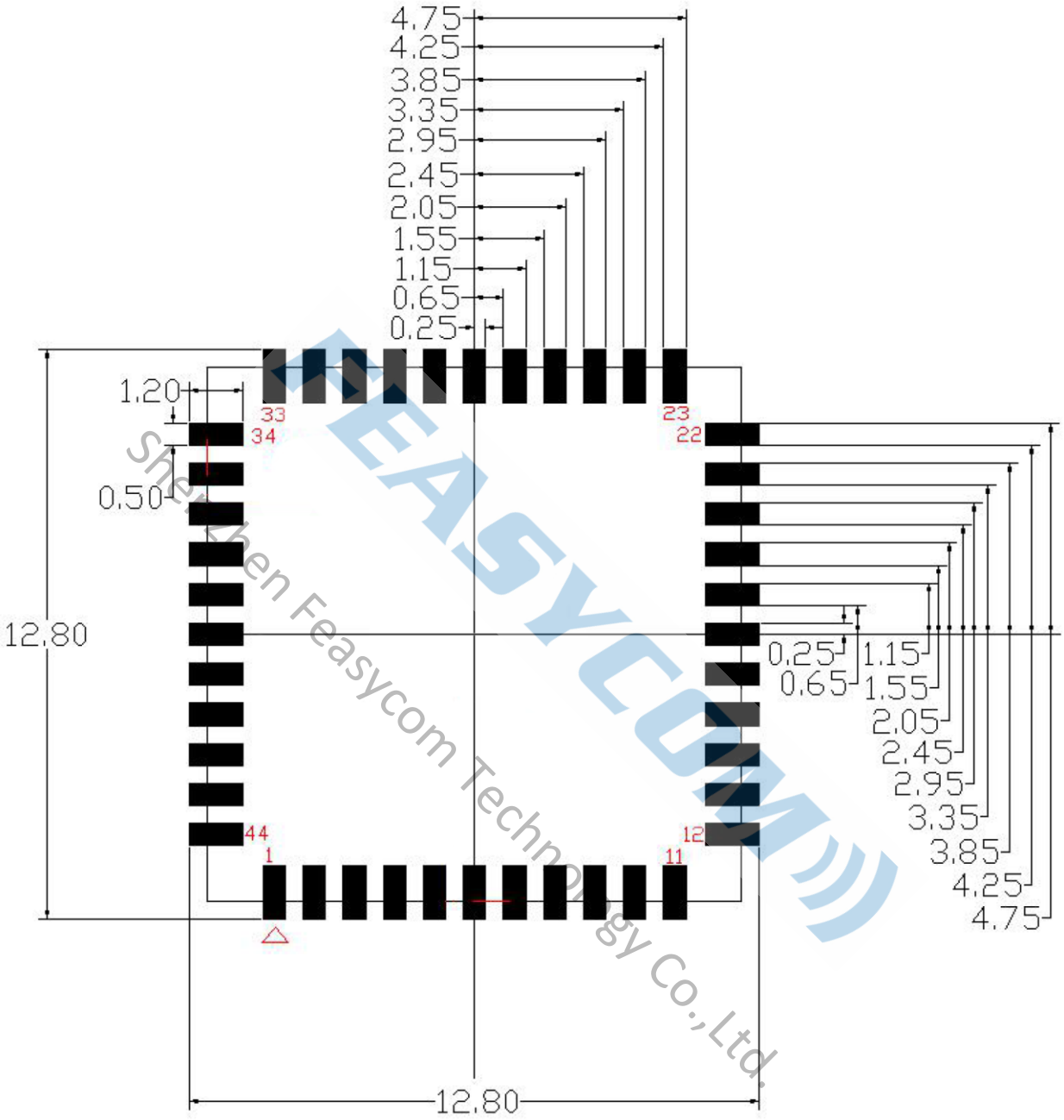


Figure 4: FSC-BW110 footprint

10. HARDWARE INTEGRATION SUGGESTIONS

10.1 Soldering Recommendations

FSC-BW110 is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of

the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

10.2 Layout Guidelines(Internal Antenna)

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.

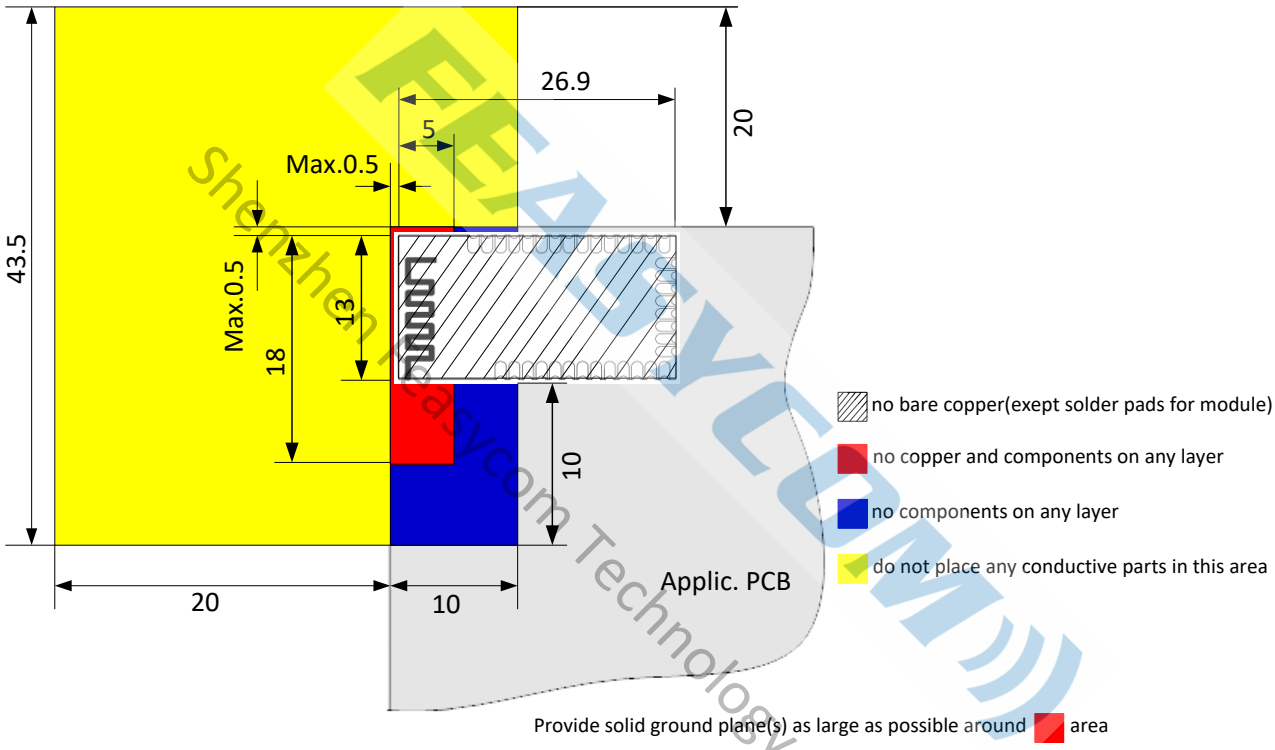


Figure 5: FSC-BW110 Restricted Area

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

10.3 Layout Guidelines(External Antenna)

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of

the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

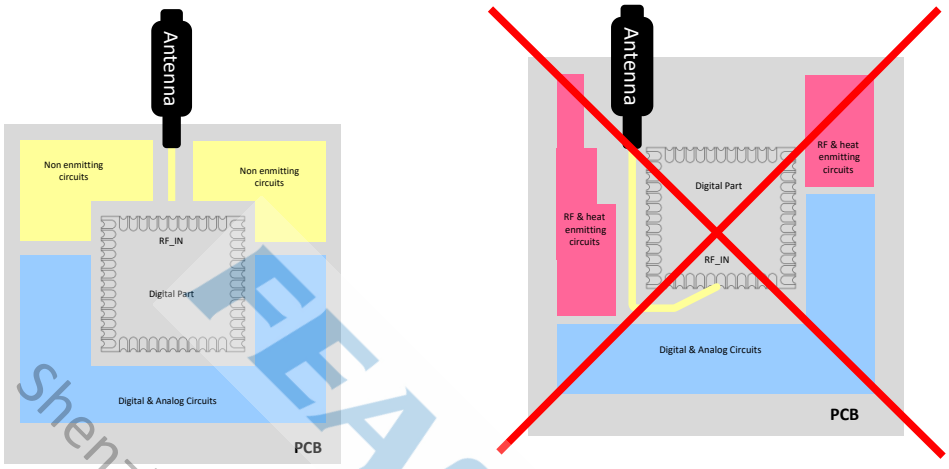


Figure 6: Placement the Module on a System Board

10.3.1 Antenna Connection and Grounding Plane Design

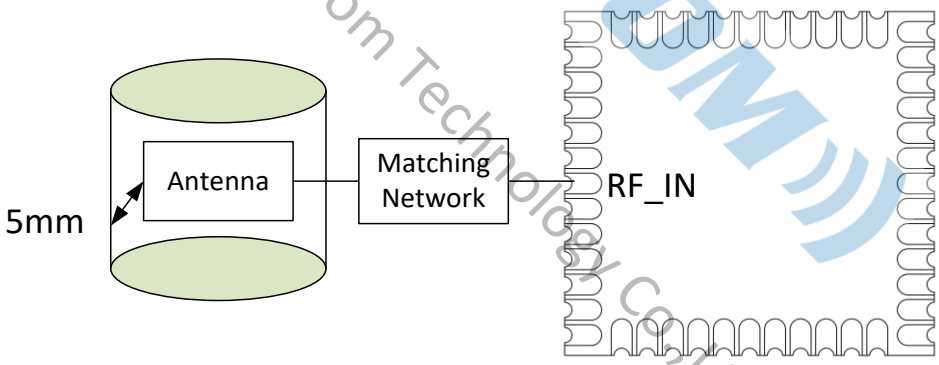


Figure 7: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

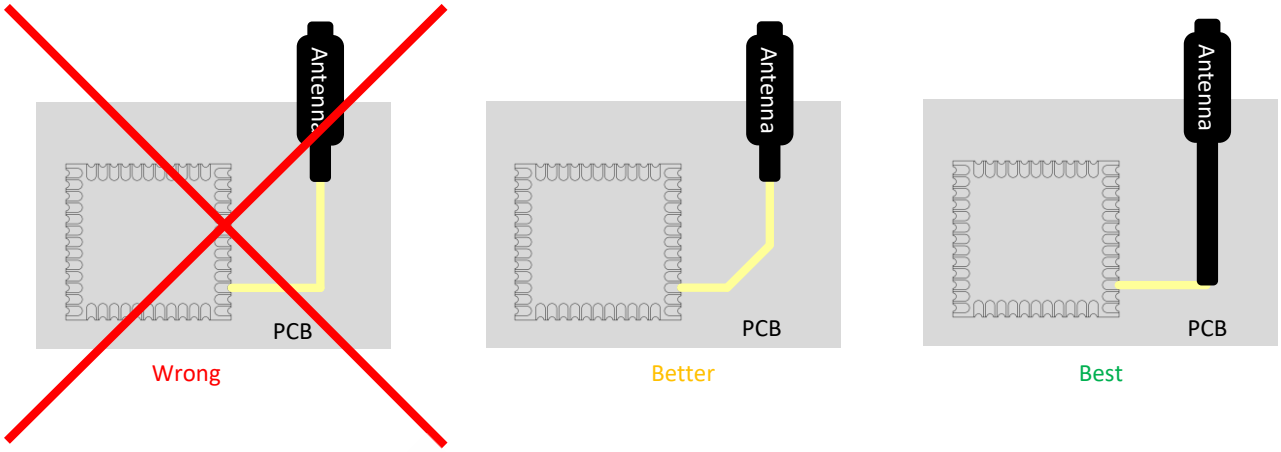


Figure 8: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

11. PRODUCT PACKAGING INFORMATION

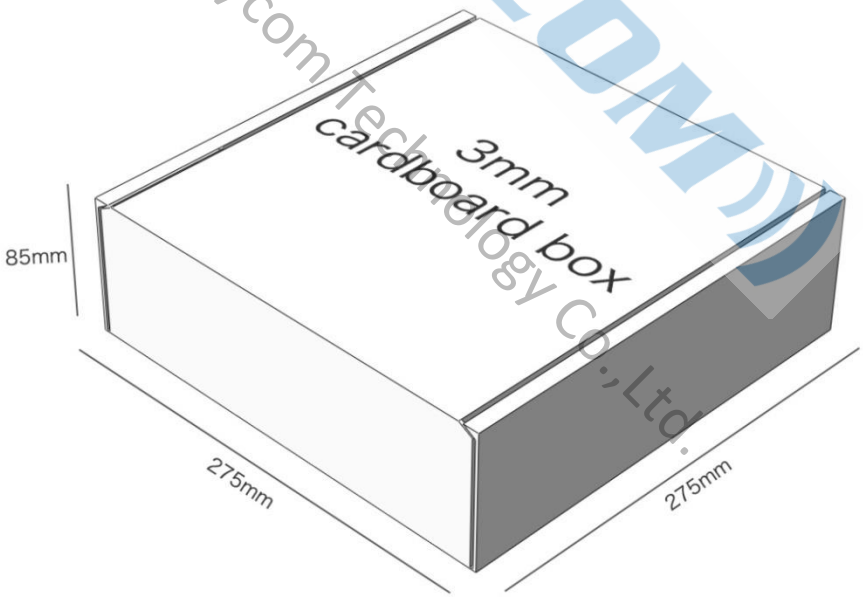
11.1 Default Packing

a, Tray vacuum

b, Tray Dimension: 180mm * 195mm

Figure 9: Tray vacuum

11.2 Packing box(Optional)



* If require any other packing, must be confirmed with customer

* Package: 1000PCS Per Carton (Min Carton Package)

Figure 10: Packing Box

12. APPLICATION SCHEMATIC