FSC-BT1057

Bluetooth 5.3 Dual Mode And LE Audio Module Datasheet

Version 1.1

Revision History

Version	Data	Notes	
1.0	2022/5/14	Initial Version	Mo
1.1	2022/5/14	Second revision Increase description such as LE Audio	Mo

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Contents

1. INTRODUCTION

Overview

FSC-BT1057 it is a Bluetooth dual-mode and LE Audio module series. It supports a Bluetooth Low Energy and compliant system for audio and data communication.

FSC-BT1057 integrates an ultra-low-power PMU and application processor with embedded flash memory, a high-performance stereo codec, Class-AB and Class-D headphone drivers , a power management subsystem, I^2S, I^2C , UART , PIO ,LED drivers and ADC I/O in a SOC IC.

Both cores use external flash to execute code, making it easy for user to differentiate products from new features without delaying the development

By default, FSC-BT1057 module is equipped with powerful and easy-to-use Feasycom firmware. It's easy to use and completely encapsulated. Feasycom firmware enables users to access Bluetooth functionality with simple ASCII commands delivered to the module over serial interface - it's just like a Bluetooth modem.

Therefore, FSC-BT1057 provides an ideal solution for developers who want to integrate Bluetooth wireless technology into their design.

Features

- Qualified to Bluetooth® v5.3 specification
- Dual 240 MHz Qualcomm® Kalimba™ audio DSPs
- 32/80 MHz Developer Processor for applications
- Firmware Processor for system
- High-performance 24-bit stereo audio interface
- Digital and analog microphone interfaces
- Flexible LED controller and LED pins with PWM support
- Serial interfaces: UART, Bit Serializer (I^2C/SPI), USB 2.0
- Advanced audio algorithms
- Active Noise Cancellation: Hybrid, Feedforward, and Feedback modes, using Digital or Analog Mics, enabled using license keys available from Qualcomm®
- Qualcomm® LE Audio, aptX™ and aptX HD Audio
- aptX Adaptive, enabled using license key
- Qualcomm® cVc™ Noise Cancellation Technology, enabled using license key
- Integrated PMU: Dual SMPS for system/digital circuits, Integrated Li-ion battery charger

Bluetooth subsystem

- Qualified to Bluetooth v5.3 specification including 2 Mbps Bluetooth Low Energy and Bluetooth Low Energy Isochronous Channels
- Qualcomm® Bluetooth High Speed Link
- Single ended antenna connection with on-chip balun and Tx/Rx switch
- Bluetooth, Bluetooth Low Energy, and mixed topologies supported
- Class 1 support

Application

- TrueWireless™ stereo earbuds
- Wired/wireless stereo headsets/headphones
- Bluetooth Speaker

1.1 Selection of version

Order Number	Descriptions	Module picture as below showing
FSC-BT1057	Chip： QCC5171	
	Chip：	

2. General Specification

Table 2-1: General Specifications

Categories	Features	Implementation
Wireless Specification	Chip	QCC5171
	Bluetooth Version	V5.3
	Frequency	2.402 - 2.480 GHz
	Transmit Power	+15 dBm (Typ VBAT=3.7V)
	Receive Sensitivity	-96.5 dBm (typ.) π/4 DQPSK receiver sensitivity -90.0 dBm (typ.) 8DPSK receiver sensitivity -100.5 dBm (typ.) BLE 1 Ms/s receiver sensitivity
		Real-time digitised RSSI available to application
	Raw Data Rates (Air)	3 Mbps (Classic BT - BR/EDR)
Host Interface and Peripherals	UART Interface	TX, RX, CTS, RTS
		General Purpose I/O
		Default 115200,N,8,1
		Baudrate support from 2400 to 4000000
	GPIO	20 (maximum – configurable) lines
		O/P drive strength (2, 4, 8, or 12 mA)
		Pull-up resistor (70 KΩ) control
	I^2C Interface	I^2C Master interface with speed up to 400 kbps
	SPI Interface	SPI debug and programming interface with read access disable locking
	ADC Interface	Analog input voltage range: 0~ 1.854V
		10-bit ADC
		4 channels (configured from AIO total)
	USB Interface	1 USB2.0 Full Speed (12 Mb/s)
	Audio CODEC	LE Audio, aptX, aptX HD, aptX Adaptive(enabled using license key) ,SBC and AAC audio codecs
		Configurable Signal Detection to trigger events
		Compander to compress or expand the dynamic range of the audio
		Post Mastering to improve DAC fidelity
		24-bit I^2S interface with 1 input and 3 output channels , Supports 8-slot

		TDM, Supports 8 kHz, 16 kHz, 32 kHz, 44.1 kHz, 48 kHz, 96 kHz, 192 kHz, 384 kHz sample rates
		SPDIF interfaces ： Two instances configurable as input or output，Supports 8 kHz, 16 kHz, 32 kHz, 44.1 kHz, 48 kHz, 96 kHz, 192 kHz sample rates
		2 coder decoder (codec) output channels, supporting 8 kHz, 16 kHz, 32 kHz, 44.1 kHz, 48 kHz, 96 kHz, 192 kHz sample rates,16 codec input channels supporting 8 kHz, 16 kHz, 32 kHz, 44.1 kHz, 48 kHz, 96 kHz sample rates
		Digital mic: Five interfaces supporting up to ten microphones, Supports 500 kHz, 571 kHz, 666 kHz, 800 kHz, 1 MHz, 1.33 MHz, 2 MHz, and 4 MHz clock frequencies
		Stereo audio ADC with line input, stereo audio DAC
		Supported sample rates of 8, 16, 32, 44.1, 48,96 ,192 and 384KHz(Input)
		MIC/Line_IN SNR: 99 dB
		MIC/Line_IN THD+N: -94.9dB
		Audio Output SNR: 103.8 dBA typ
		Audio Output THD+N: -92.5dB typ
		Audio Output Power: 1000mV (typ)(0dBFS 10K load)
Profiles	BR/EDR	SPP (Serial Port Profile) - Up to 600 Kbps
		A2DP/AVRCP/HFP/HSP/HOGP/PBAP/SPP Profiles support
	Bluetooth Low Energy	GATT Client & Peripheral
		Simultaneous BR/EDR and BLE support
Maximum Connections	BR/EDR	up to 7 active slaves
	Bluetooth Low Energy	1 connection as peripheral , up to 5 connections as central
FW upgrade		Via UART(TBD)
		USB(TBD)
		OTA
		SPI
Supply Voltage	Supply	VDD_IO: 1.7 ~ 3.3V; VBAT_IN: 2.8V~ 4.30V
Power Consumption （Load=10KΩ,VBAT_IN=3.3V）		Play：<5mA（0dB 1KHz sine wave signal）---*Average
		Pairing： <5mA---*Average
		OFF： <100uA---*Average
Physical	Dimensions	13mm(W) X 26.9mm(L) X 2.2mm(H); Pad Pitch 1mm
Environmental	Operating	-40°C to +85°C
	Storage	-40°C to +85°C
Miscellaneous	Lead Free	Lead-free and RoHS compliant
	Warranty	One Year
Humidity		10% ~ 90% non-condensing
MSL grade:		MSL 3
ESD grade:		Human Body Model: Class 2 2kV (all pins)
		Charged Device Model: Class III 500 V (all pins)

3. HARDWARE SPECIFICATION

3.1 Block Diagram and PIN Diagram

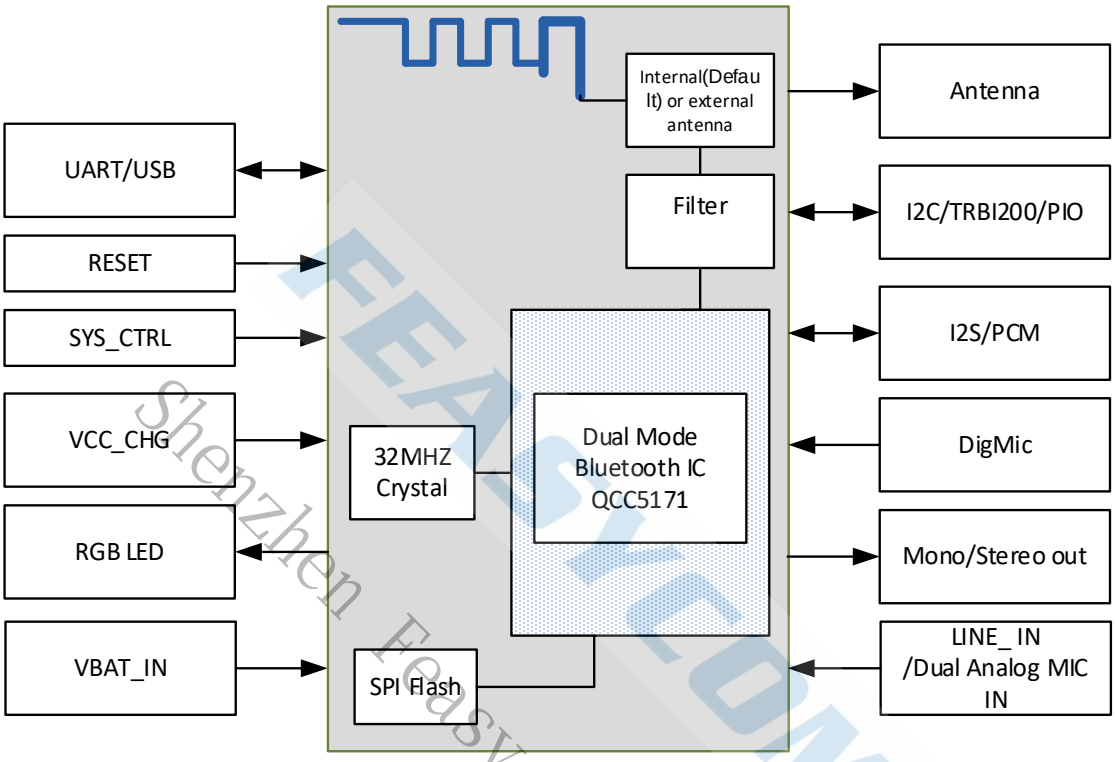

Figure 3-1: Block Diagram

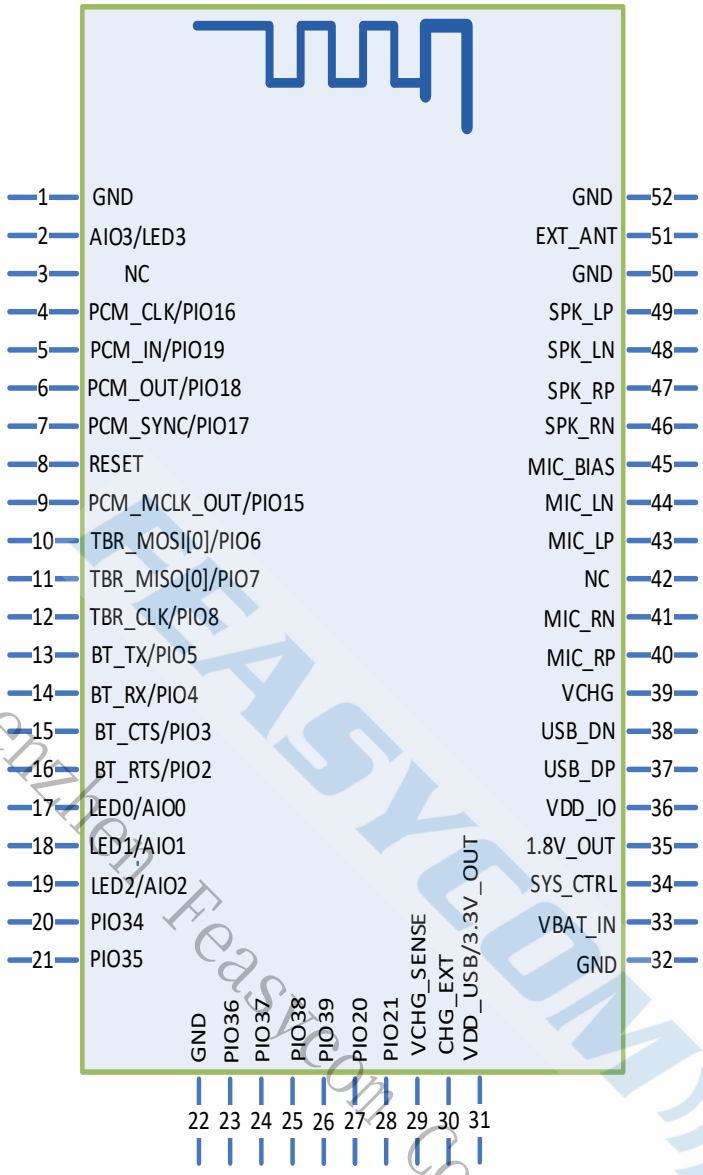

Figure 3-2: FSC-BT1057 PIN Diagram(Top View)

3.2 PIN Definition Descriptions

Table 3-1: Pin definition

Pin	Pin Name	Type	Pin Descriptions	Notes
1	GND	Vss	Power Ground	
2	AIO3/LED3	A,I/O	General-purpose analog/digital input or open drain LED output.	
3	NC	NC	NC-Do Not GND	
4	PCM_CLK/PIO16	I/O	Programmable I/O line 16. Alternative function: PCM_CLK	Note 6
5	PCM_IN/PIO19	I/O	Programmable I/O line 19. Alternative function: PCM_DIN[0]	Note 6
6	PCM_OUT/PIO18	I/O	Programmable I/O line 18. Alternative function: PCM_DOUT[0]	Note 6

7	PCM_SYNC/PIO17	I/O	Programmable I/O line 17. Alternative function: PCM_SYNC	Note 6
8	RESET	I/O	Automatically defaults to RESET# mode when the device is unpowered, or in off modes. Reconfigurable as a PIO after boot.	
9	PCM_MCLK_OUT/PIO15	I/O	Programmable I/O line 15. Alternative function: MCLK_OUT	
10	PIO6	I/O	Programmable I/O line 6. Alternative function: TBR_MOSI[0]	
11	PIO7	I/O	Programmable I/O line 7. Alternative function: TBR_MISO[0]	
12	PIO8	I/O	Programmable I/O line 8. Alternative function: TBR_CLK	
13	BT_TX/PIO5	I/O	BT_TX /Programmable I/O line 5. Alternative function: TBR_MISO[1]	Note 6
14	BT_RX/PIO4	I/O	BT_RX/Programmable I/O line 4. Alternative function: TBR_MOSI[1]	Note 6
15	BT_CTS/PIO3	I/O	BT_CTS/Programmable I/O line 3	Note 6
16	BT_RTS/PIO2	I/O	BT_RTS/Programmable I/O line 2	Note 6
17	AIO0/LED0	A,I/O	General-purpose analog/digital input or open drain LED output.	Note 6,8
18	AIO1/LED1	A,I/O	General-purpose analog/digital input or open drain LED output.	Note 6,8
19	AIO2/LED2	A,I/O	General-purpose analog/digital input or open drain LED output.	Note 6,8
20	PIO34	I/O	Programmable I/O line 34	
21	PIO35	I/O	Programmable I/O line 35	
22	GND	Vss	Power Ground	
23	PIO36	I/O	Programmable I/O line 36	
24	PIO37	I/O	Programmable I/O line 37	
25	PIO38	I/O	Programmable I/O line 38	
26	PIO39	I/O	Programmable I/O line 39	
27	PIO20	I/O	Programmable I/O line 20. Alternative function: PCM_DOUT[1]	Note 5
28	PIO21	I/O	Programmable I/O line 21. Alternative function: PCM_DOUT[2]	Note 5
29	VCHG_SENSE		Charger input sense pin after external mode sense-resistor. High impedance. NOTE: If using internal charger or no charger, connect VCHG_SENSE direct to VCHG.	
30	CHG_EXT		External charger transistor current control. Connect to base of external charger transistor as per application schematic.	
31	VDD_USB/3.3V_OUT		3.3V voltage output (MAX. 50mA OUT)	Note 7

32	GND	Vss	Power Ground	
33	VBAT_IN	Vdd	Battery voltage input.	
34	SYS_CTRL	I	Typically connected to an ON/OFF push button. Boots device in response to a button press when power is still present from battery and/or charger but software has placed the device in the OFF or DORMANT state. Additionally useable as a digital input in normal operation. No pull.	Note 3
35	1.8V_OUT	Vdd	1.8V voltage output	Note 1
36	VDD_IO	I	PIO supply(1.8 V~3.3V)	Note 2
37	USB_DP		USB Full Speed device D+ I/O. IEC-61000-4-2 (device level) ESD Protection	Note 4
38	USB_DN		USB Full Speed device D- I/O. IEC-61000-4-2 (device level) ESD Protection	Note 4
39	VCHG	Vdd	Charger input to Bypass regulator.	Note 4
40	MIC_RP	A	Microphone differential 2 input, positive. Alternative function: Differential audio line input right, positive	
41	MIC_RN	A	Microphone differential 2 input, negative. Alternative function: Differential audio line input right, negative	
42	NC			
43	MIC_LP	A	Microphone differential 1 input, positive. Alternative function: Differential audio line input left, positive	
44	MIC_LN	A	Microphone differential 1 input, negative. Alternative function: Differential audio line input left, negative	
45	MIC_BIAS	Vdd	Mic bias output.	
46	SPK_RN	A	speaker differential output, negative. Alternative function: Differential line output, negative	
47	SPK_RP	A	speaker differential output, positive. Alternative function: Differential line output, positive	
48	SPK_LN	A	speaker differential output, negative. Alternative function: Differential line output, negative	
49	SPK_LP	A	speaker differential output, positive. Alternative function: Differential line output, positive	
50	GND	Vss	Power Ground	
51	RF_OUT	RF	Bluetooth transmit/receive.	Note 9
52	GND	Vss	Power Ground	

Module Pin Notes:

Note 1	The internal output of 1.8 V power supply provides maximum 30mA current, and the specific use method can see the application circuit diagram
Note 2	Provid voltage reference to I/O, such as： PIO, UART, SPI, I^2S, PCM,etc
Note 3	Regulator enable input. Can also be sensed as an input. Regulator enable and multifunction button. A high input (tolerant to VBAT) enables the on-chip regulators,

	which can then be latched on internally and the button used as a multifunction input. * Reset this pin for at least 100ms after VBAT_IN and VDD_IO is up, then set this pin for more than 100 ms (can use MCU/button/delayed circuit to achieve this) to start the system.
Note 4	Using USB function and Lithium battery charging function, the pin should connect 5V voltage
Note 5	1, Alternate I^2C function 2, I^2C Serial Clock and Data. It is essential to remember that pull-up resistors on both SCL and SDA lines are not provided in the module and MUST be provided external to the module.
Note 6	For customized module, this pin can be work as I/O Interface.
Note 7	1, When the Pin33(BAT_IN) with a 3V3~4V2 this pin outputs 2V8 ~ 3V0 (maximum current: 50mA) 2, when the No. 39 PIN (VCHG) with a 5V input pin, this pin outputs 3.2V ~ 3.4V (maximum current: 50mA)
Note 8	Analog input voltage range: 0~ 1.8V
Note 9	By default, this PIN is an empty feet. This PIN can connect to an external antenna to improve the Bluetooth signal coverage. To use an external antenna, the position of an 0Ω resistor needs to be changed to disconnect the on-board antenna and connect to the external antenna; Or contact Feasycom for modification.

4. PHYSICAL INTERFACE

4.1 Power Management

4.1.1 Power Supply

- The transient response of the regulator is important. If the power rails of the module are supplied from an external voltage source, the transient response of any regulator used should be 20μs or less. It is essential that the power rail recovers quickly.

4.1.2 Battery Charger

- The default mode for the FSC-BT1057 battery charger is OFF.
- The internal charger circuit can provide up to 200mA of charge current.

The battery charger operating mode is determined by the battery voltage and current, see the table below and the picture below.

4.1.2.1 General charger operation

The charger system has five main operating states. The current charger status can be read by application software. Figure 4-1 shows the five states in the charge cycle.

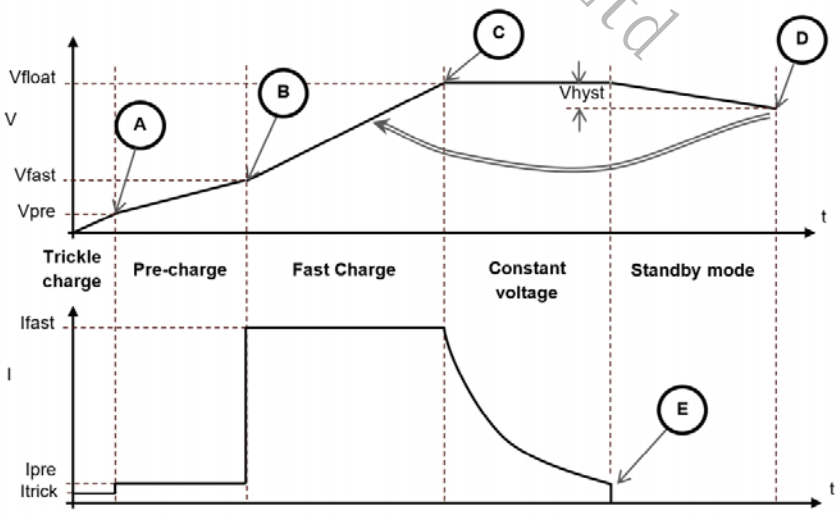

Figure 4-1: Charge cycle states

Trickle Charge

This mode is entered when VBAT is sensed in the range 0 to Vpre. This is encountered only with a deeply discharged battery (below Vpre threshold, point (A), or when the cell's battery protection circuit has opened, temporarily disconnecting the cell. It is used to pass a small charging current to safely charge a cell, and also cause a cell battery protection circuit to reset. .

The hysteresis on Trickle charge into Pre-Charge is typically 100 mV.

Pre Charge

This mode is entered when VBAT is sensed in the range Vpre to Vfast. In this range, it is not recommended to charge the cell at maximum rate, but a faster charge rate than that of Trickle charge is allowable. Typically this is ~10 % to 20 % of the Fast charge rate. The Vfast threshold, point (B) is programmable.

The hysteresis on the Vfast transition from Pre-Charge to Fast charge is typically 200 mV

Fast Charge Mode

Fast charge has two parts:

- **Constant current**: Entered when VBAT is sensed in the range Vfast to Vfloat point (C). This is the maximum charge rate, and should be set according to the battery manufacturers Data Sheet.
- **Constant voltage**: When Vfloat is reached the cell voltage is maintained at Vfloat, and the current slowly reduces until the termination point (E) is reached where charging ceases, and the charger transitions to Standby mode.

Vfloat can be configured from 3.65 V to 4.40 V in 50 mV increments. This allows use of cells with different Vfloat values, or cell life extension by reducing Vfloat. Vfloat can also be altered depending on temperature change, for cell life protection.

The current termination point (E) can be adversely influenced by dynamic changes in VBAT load current, or to a lesser extent changes in VCHG voltage.

Standby Mode

Once the charge current has fallen and the charger is terminated, the system enters Standby mode. In Standby mode, the charger does not charge. It continues to monitor the battery voltage. If the voltage falls back below Vfloat by more than a configurable threshold Vhyst, point (D), then the charger re-enters Fast charge mode. Vhyst is expressed as a percentage of Vfloat.

4.1.2.2 Battery protection

Deeply discharging a Li-ion battery for a long time can cause irreversible damage, leading to excessive heating on a subsequent charger cycle.

To prevent this, customer application software should turn off the device at ~3.0 V. Typically cells have ~5 % usable capacity left at this point.

QTIL strongly recommends that all applications include a battery protection IC, normally built into the battery pack itself, as a secondary level of protection. This protection typically disconnects the battery cell if the voltage drops too low, or goes too high, and protects against overcurrent in the connections between FSC-BT1057 and the cell itself.

4.2 PIO

FSC-BT1057 has the following digital I/O pads:

- 17 PIO pads
- 4 x pads intended for LED operation: LED[3:0]
- 1 x Power-on signaling: SYS_CTRL, usable as an input after boot.

4.3 PIO pad allocation

The following FSC-BT1057 functions have specific pad allocations:

- LED pads
- Transaction bridge
- Audio I²S/PCM

NOTE

Digital microphones, UART, Bit Serializer (I²C/SPI), SPDIF and LED PWM controllers can use any PIO.

4.4 Standard PIO

The standard digital I/O pins (PIO) on FSC-BT1057 are split into separate pad domains. Each VDD_IO domain can be separately powered, from 1.7 V to 3.6 V. When PIOs in a supply domain are used for a high-speed interface, decoupling the respective VDD_IO pin with a 100 nF decoupling capacitor may be beneficial. The VDD_IO of a particular pin should be powered before voltages are applied to any PIO powered by that domain, otherwise back powering can occur through the electrostatic discharge (ESD) protection in the pad.

PIO can be programmed to have a pull-up or pull down with two strengths (weak and strong). PIO can also be programmed with a sticky function where they are strongly pulled to their current input state. PIO have a reset pull state, after reset the pulls can be re-configured by software.

PIO also have a programmable drive strength capability of 2, 4, 8, or 12 mA.

All PIO are readable by all subsystems, but for write access are assigned by software to particular subsystem control. PIO inputs are via Schmitt triggers.

4.5 Reset

FSC-BT1057 is digital reset pin (RESET#) is an active low reset signal.

The pin is active low and on-chip glitch filtering avoids the need to filter out any spurious noise that may cause unintended resets. The RESET# pin has a fixed strong pull-up to VDD_IO, and therefore can be left unconnected. The input is asynchronous, and is pulse extended within FSC-BT1057 to ensure a full reset

FSC-BT1057 contains internal Reset Protection functionality to automatically keep the power rails enabled and enable the system to restart after unintended reset (such as a severe ESD event). Assertion of RESET# beyond the Reset Protection timeout (typically greater than ~1.8 s) causes the device to power down if VCHG is not present and SYS_CTRL is low. FSC-BT1057 then requires a SYS_CTRL assertion or VCHG attach to restart.

NOTE

- FSC-BT1057 is always powered if VCHG is present. It does not power down if RESET# is asserted while VCHG remains present.
- QTIL recommends that FSC-BT1057 is powered down via software-controlled methods rather than external assertion of RESET#.
- Holding RESET# low continuously is not the lowest FSC-BT1057 power state, because pull downs are enabled on VCHG and VDD_USB in this state.
- RESET# is guaranteed to work if held low for 120 µs

4.6 SYS_CTRL pin

- SYS_CTRL is an input pin that acts as a power on signal for the internal regulators.
- From the OFF state, SYS_CTRL must be asserted for >20 ms to start power up.
- SYS_CTRL is VBAT tolerant (4.8 V max), and typically connected via a button to VBAT. SYS_CTRL has no internal pull resistor, and requires an external pull-down if left undriven.
- Use software to logically disconnect SYS_CTRL from the power on signal for internal regulators. For example, when booted, software takes control of the internal regulators and the state of SYS_CTRL is ignored by the regulators.

4.7 RF Interface

For this module, the antenna must be connected to work properly.

The user can connect a 50ohm antenna directly to the RF port.

- 2402–2480 MHz Bluetooth 5.3 Dual Mode (BT and BLE); 1 Mbps to 3 Mbps over the air data rate.
- TX output power of +15dBm (MAX).
- Receiver to achieve best sensitivity -100.5dBm for BLE and -97dBm for Classic Bluetooth.

4.8 Serial Interfaces

4.8.1 UART Interface

FSC-BT1057 provides one channels of Universal Asynchronous Receiver/Transmitters(UART)(Full-duplex asynchronous communications). The UART Controller performs a serial-to-parallel conversion on data received from the peripheral and a parallel-to-serial conversion on data transmitted from the CPU. Each UART Controller channel supports ten types of interrupts.

This is a standard UART interface for communicating with other serial devices. The UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

When the module is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators.

This module output is at 3.3V CMOS logic levels (tracks VCC). Level conversion must be added to interface with an RS-232 level compliant interface.

Some serial implementations link CTS and RTS to remove the need for handshaking. We do not recommend linking CTS and RTS except for testing and prototyping. If these pins are linked and the host sends data when the FSC-BT1057 deasserts its RTS signal, there is significant risk that internal receive buffers will overflow, which could lead to an internal processor crash. This drops the connection and may require a power cycle to reset the module. We recommend that you adhere to the correct CTS/RTS handshaking protocol for proper operation.

Table 4-1: Possible UART Settings

Parameter		Possible Values
Baudrate	Minimum	2400 baud (≤2%Error)
	Standard	19200bps(≤1%Error)
	Maximum	4Mbaud(≤1%Error)
Flow control		RTS/CTS, or None
Parity		None, Odd or Even
Number of stop bits		1 /2
Bits per channel		8

When connecting the module to a host, please make sure to follow .

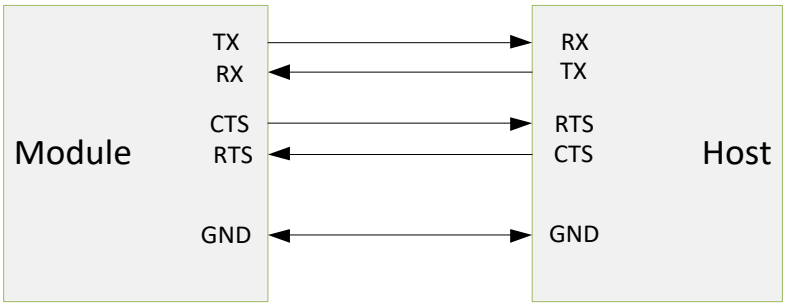

Figure 4-2: UART Connection

The UART interface resets FSC-BT1057 on reception of a break signal. A break is identified by a continuous logic low (0V) on the UART_RX terminal, as below picture shows. If t_{BRK} is longer than the value defined by the PSKEY_HOSTIO_ UART _RESET_TIMEOUT, a reset occurs. This feature enables a host to initialise the system to a known state. Also, FSC-BT1057 can issue a break character for waking the host.

Figure 4-3: Break Signal

The UART interface is tristate while FSC-BT1057 is being held in reset. This enables the user to connect other devices onto the physical UART bus. The restriction with this method is that any devices connected to this bus must tristate when FSC-BT1057 reset is de-asserted and the firmware begins to run.

4.8.2 I²C Interface

FSC-BT1057 includes a configurable I²C interface.

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

Data is transferred between a Master and a Slave synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8-bit long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to the following figure for more details about I²C Bus Timing.

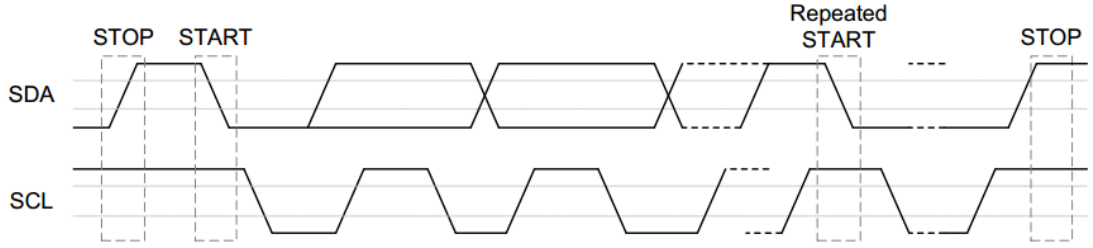

Figure 4-4: I2C Bus Timing

The device on-chip I²C logic provides the serial interface that meets the I²C bus standard mode specification. The I²C port handles byte transfers autonomously. The I²C H/W interfaces to the I²C bus via two pins: SDA and SCL. Pull up resistor is needed for I²C operation as these are open drain pins. When the I/O pins are used as I²C port, user must set the pins function to I²C in advance.

4.8.3 USB Interface

- FSC-BT1057 has a USB device interface: An upstream port, for connection to a host Phone/PC or battery charging adaptor. For details software support for USB features, refer to ADK documentation.
- The device port is a USB2.0 Full Speed (12 Mb/s) port. Typically FSC-BT1057 enumerates as a compound device with a hub with the enabled audio source / sink / HID / mass storage device appearing behind this hub.
- The DP 1.5 k pull-up is integrated in FSC-BT1057. No series resistors are required on the USB data lines.
- FSC-BT1057 contains integrated ESD protection on the data lines to IEC 61000-4-2 (device level). In normal applications, no external ESD protection is required.
- Extra ESD protection is not required on VCHG (VBUS) because FSC-BT1057 meets the USB certification requirements of a minimum of 1uF, and a maximum of 10 µF being present on VCHG (VBUS).
- The VCHG input of FSC-BT1057 is tolerant of a constant 6.5 V and transients up to 7.0 V. If extra overvoltage protection is required, external clamping protection devices can be used.
- FSC-BT1057 supports charger detection to the USB BC 1.2 specification.

4.8.4 SPI master

Bitserial operating as a SPI master.

Figure 4-5 and **Figure 4-6** show bitserial interface timings with different clock phase (CPHA).

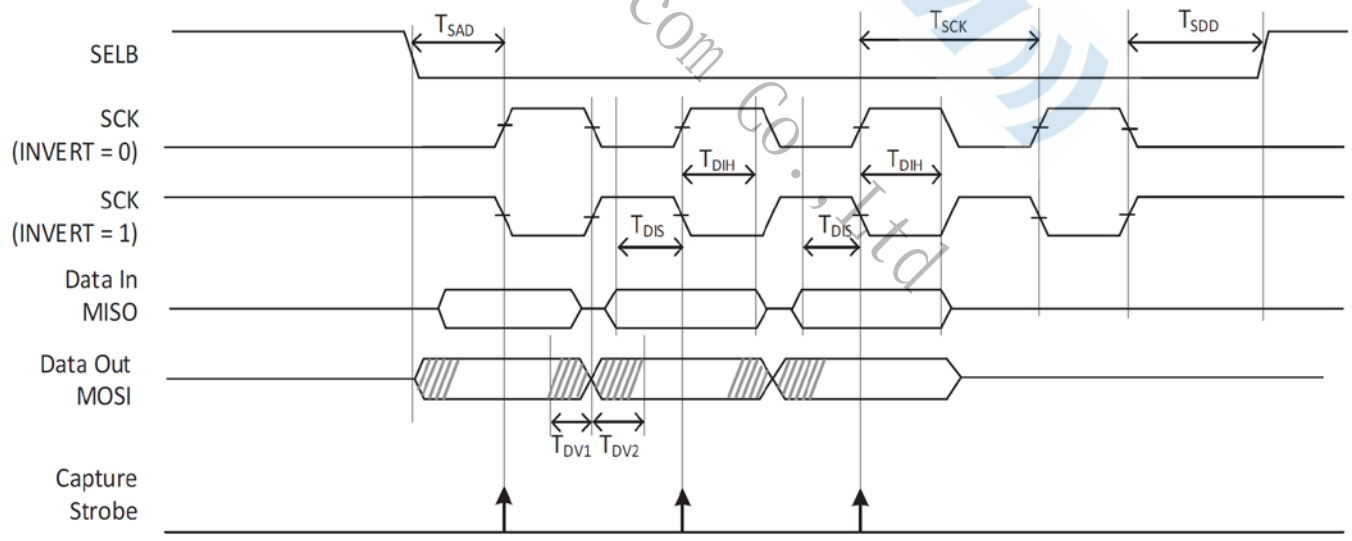

Figure 4-5 Bitserial M-SPI timing diagram, operating modes with CPHA = 0

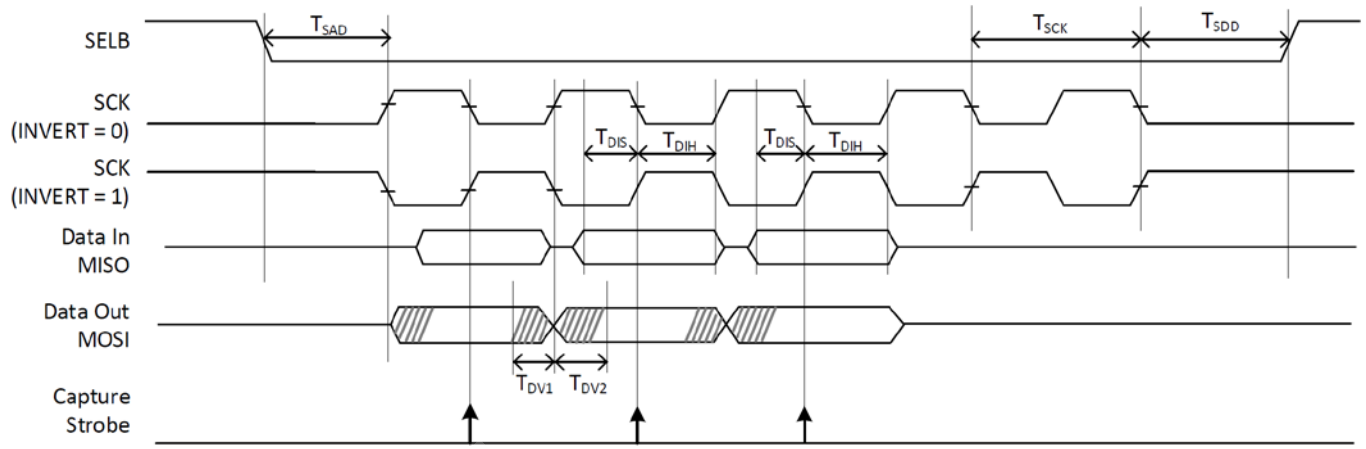

Figure 4-6 Bitserial M-SPI timing diagram, operating modes with CPHA = 1

Table **4-2** lists bitserial interface timing parameters.

Table 4-2 Bitserial M-SPI timing parameters

Parameter	Symbol	Min	Max	Unit	Notes
Clock period	TSCK	125	2000	ns	-
Sel Assert to SCK rise delay	TSAD	17.0	-	ns	-
SCK fall to SEL de-assert delay	TSDD	52.5	-	ns	-
MISO data setup	TDIS	39.0	-	ns	-
MISO data hold	TDIH	0.0	-	ns	-
MOSI data invalid minimum	TDV1	-13.0	-	ns	Total data invalid window of 28.1 ns
MOSI data invalid maximum	TDV2	-	15.1	ns	Total data invalid window of 28.1 ns

When operating as a SPI master the Bitserial is clocked at half the crystal frequency. SCK frequencies are integer divisions of the Bitserial clock frequency with a minimum supported division of 2. With a 32 MHz crystal the possible SCK frequencies are 8 MHz, 5.33 MHz, 4 MHz and so on.

4.9 LED Drivers

- LED Driver: This mode is designed for driving LEDs. The pad operates as an open-drain pad, tolerable of voltages up to 6.5 V. Therefore the cathode of the LED should be connected to the FSC-BT1057 LED pad. Each pad is rated to sink up to 50 mA of current.
- FSC-BT1057 has six PWM-based LED controllers controlled by the Applications subsystem. Use them for driving either the LED pads (through virtual PIOs) or other available PIOs.
- An application may configure the LED flash rate and ramp time using a dedicated API.
- Once configured, the LED flash and ramp rate are fully hardware controlled within the LED/PWM module. It is possible to synchronize any number of the LED drivers together. Use the flash/ramp rate configuration to generate color change sequences on RGB LEDs.

4.10 Audio subsystem

Audio subsystem features include:

- Analog DAC: Mono analog output configurable as differential Class-AB audio output or differential high efficiency Class-D
- Analog ADC: Stereo analog inputs configurable as single ended line inputs, or unbalanced, or balanced analog microphone inputs
- I²S/PCM interface
  - ☐ 24-bit I²S interface with 1 input and 3 output channels
  - ☐ Supports 8-slot TDM
  - ☐it I²S interfaceDMwith 1 input and 3 o,384 kHz sample rates
- SPDIF interfaces
  - ☐sTwo instances configurable as input or output
  - ☐iSupports 8, 16, 32, 44.1, 48, 96, 192 kHz sample rates
- Audio MCLK: Programmable, available on PIO[15]
- Audio engine
  - ☐u2 Codec output channels, supporting 8, 16, 32, 44.1, 48, 96, 192 kHz sample rates
  - ☐o16 Codec input channels supporting 8, 16, 32, 44.1, 48, 96 kHz sample rates
- Digital mics
  - ☐iFive interfaces supporting up to ten microphones
  - ☐oSupports 500 kHz, 571 kHz, 666 kHz, 800 kHz, 1 MHz, 1.33 MHz, 2 MHz, and 4 MHz clock frequencies
- 1 or 2-mic cVc headset noise reduction and echo cancellation technology
- SBC and AAC audio codecs support
- aptX, aptX HD, aptX Adaptive, enabled using license key
- ANC: Hybrid, Feedforward, and Feedback modes

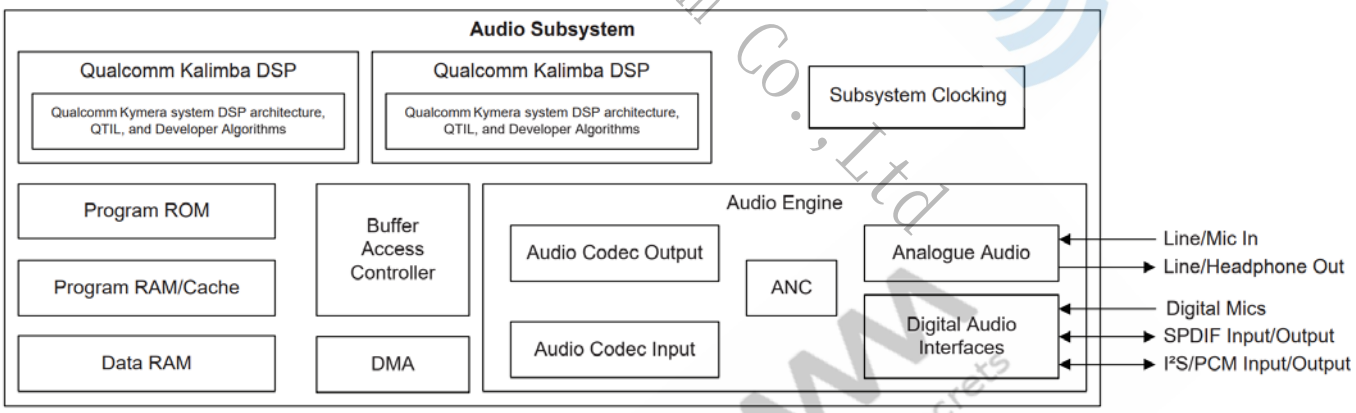

Figure 4-7: Audio subsystem

4.10.1 Audio engine

The Audio subsystem implements 16 input and 2 output codec channels for the digital and analog audio interfaces. The subsystem also implements Active Noise Cancellation hardware.

Audio Codec Block Diagram

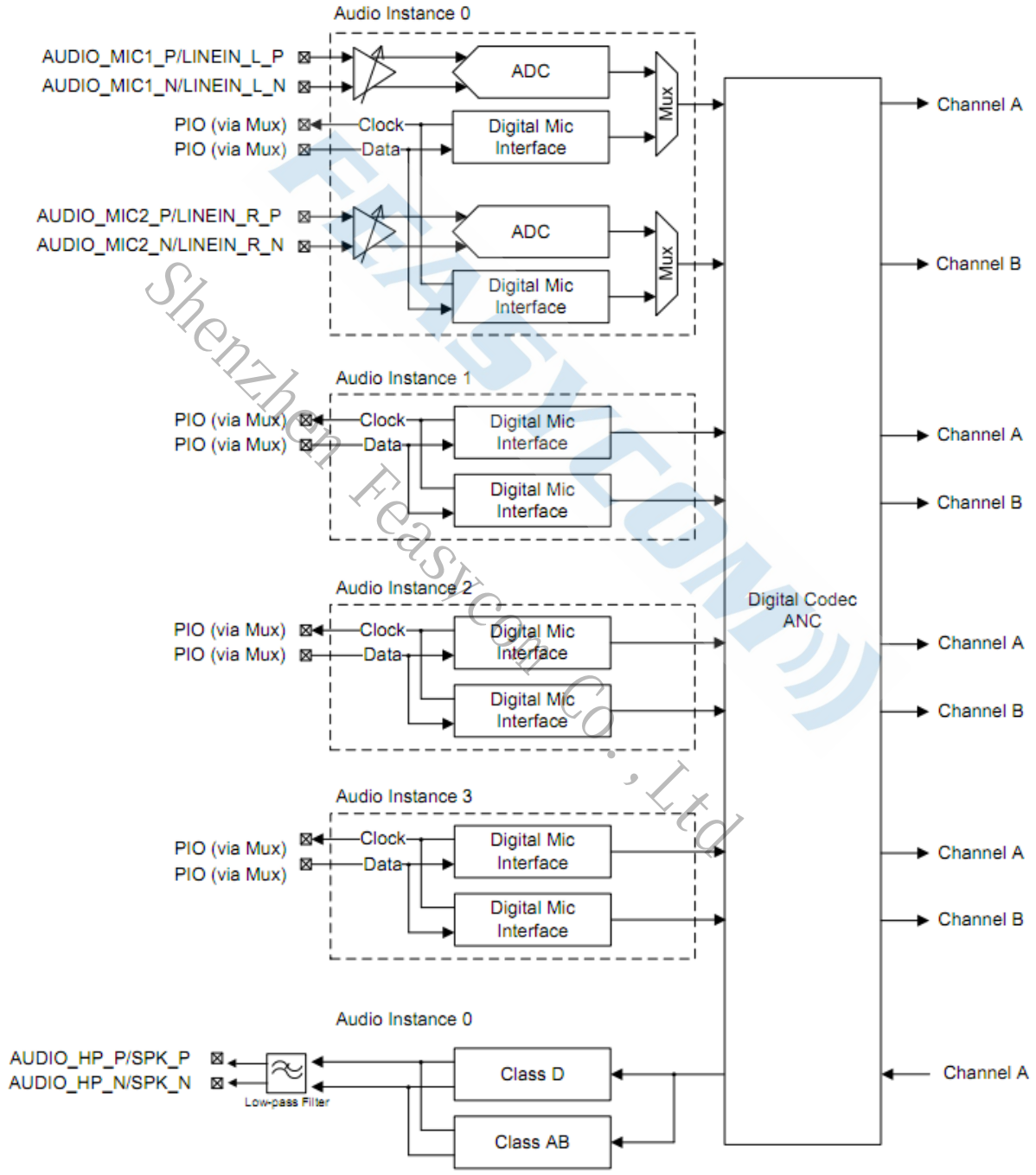

Figure 4-8: FSC-BT1057 analog audio and microphone interfaces

NOTE: FSC-BT1057 does not support 16/32 ohm headphones

4.10.2 Line/Mic inputs

FSC-BT1057 has two high-quality audio input ADCs (HQADC), primarily intended for line input use, but also suitable for other applications that support mixed differential and single ended use cases. The ADC is 24-bit, and capable of sample rates from 8 kHz to 96 kHz. The HQADC is configurable, with an internal switch arrangement, see **Figure 4-9**. VAG is a virtual ground reference. The software API allows for direct control of the nine switches, or a simpler control, supporting three standard modes:

- Stereo differential input
- Stereo single ended input, using the P inputs
- Stereo single ended input, using the N inputs

Inputs should be AC coupled, typically with a 2u2 capacitor. This capacitor value can be reduced at the expense of low frequency response attenuation.

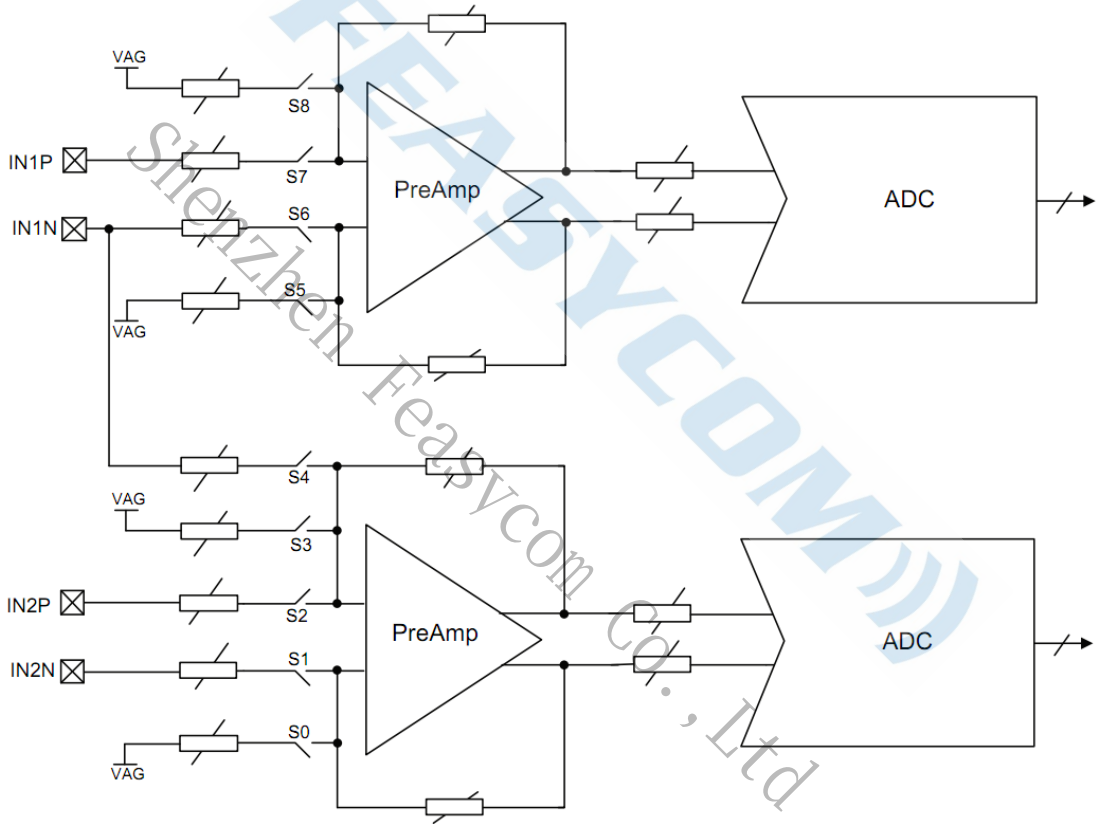

Figure 4-9:FSC-BT1057 high-quality ADC input switch configuration

4.10.3 Line/Headphone outputs

A high-quality audio output DACs (HQDAC) drive mono low impedance differential loads (BTL headphones) or Line out.

The HQDAC supports two modes of operation. Class-D is a high efficiency, switching mode amplifier. The secondary Class-AB is a linear amplifier and consumes more power.

4.10.4 Standard I²S/PCM interface

FSC-BT1057 provides a standard I²S/PCM interface capable of operating at up to a 384 kHz sample rate.

The I²S/PCM port is highly configurable with alternate PCM modes, and has the following options:

- SYNC edge position selectable to align with start of channel data (PCM mode), or 1 clock before start of channel data (I²S mode)
- Master (generate CLK and SYNC) or Slave (receive CLK and SYNC) (PCM/IM m
- SYNC polarity (PCM)
- Long or short SYNC (PCM)
- Left or right justification (PCM/ISla
- Sign extension / zero pad (PCM)
- Optional tri-state at end of word (PCM)
- Optional invert of clock (PCM/ Id (
- 13/16/24-bit per sample (PCM/ IId
- Up to four slots per frame (PCM)

Table 4-3: Alternative functions of the digital audio bus interface on the PCM interface

I²S Pin	PCM function	Description
I2S _ DIN /SDIN/ADCDAT	PCM _DIN	Data intput
I2S _DOUT / SDOUT / DACDAT	PCM_DOUT	Data output
I2S_FS / WS / LRCLK	PCM_SYNC	Word sync
I2S _CLK / SCK / BCLK	PCM_CLK	Bit clock

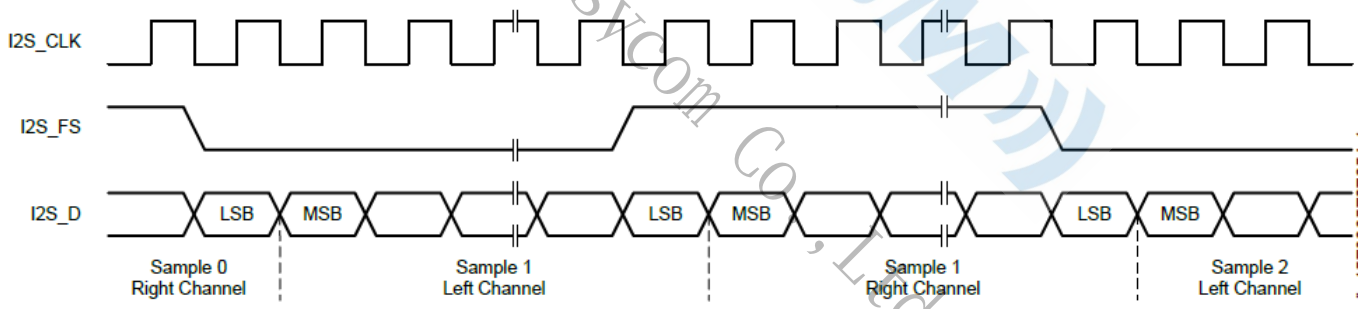

Figure 4-10:I²S general format

Table 4-4: Digital audio interface slave timing

Parameter	Min	Type	Max	Unit
$t_{hsclksynch}$ - Hold time from PCM_CLK low to PCM_SYNC high	5	-	-	ns
$t_{susclksynch}$ - Set-up time for PCM_SYNC high to PCM_CLK low	15	-	-	ns
$t_{supinsclkl}$ - Set-up time for PCM_IN valid to PCM_CLK low	15	-	-	ns
$t_{hpinsclkl}$ - Hold time for PCM_CLK low to PCM_IN invalid	5	-	-	ns

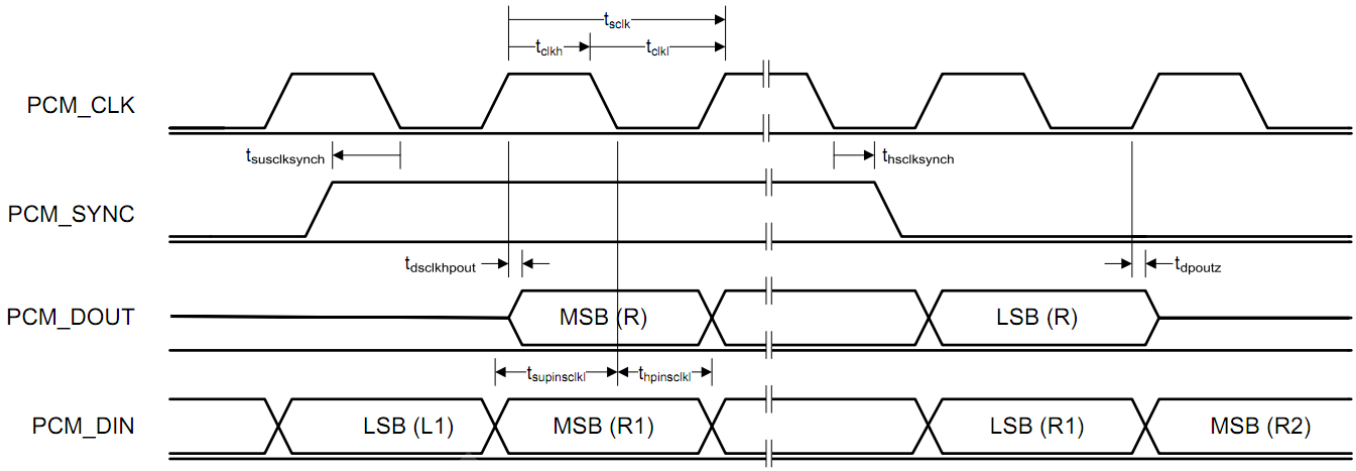

Figure 4-11: Digital audio interface slave timing

Table 4-5:I²S/PCM master mode timing parameters, WS and SCK as outputs

Parameter	Min	Type	Max	Unit
$t_{dmclksynch}$ - Delay time from PCM_CLK high to PCM_SYNC high	-	-	20	ns
$t_{dmclkpout}$ - Delay time from PCM_CLK high to valid PCM_OUT	-		20	ns
$t_{dmclkhsyncl}$ -Delay time from PCM_CLK high to PCM_SYNC low	-	-	20	ns
$t_{dmclkhpoutz}$ -Delay time from PCM_CLK high to PCM_OUT high impedance	-	-	20	ns
$t_{supinclkl}$ - Set-up time for PCM_IN valid to PCM_CLK low	-	-	20	ns
$t_{hpinclkl}$ - Hold time for PCM_CLK low to PCM_IN invalid	0	-	-	ns

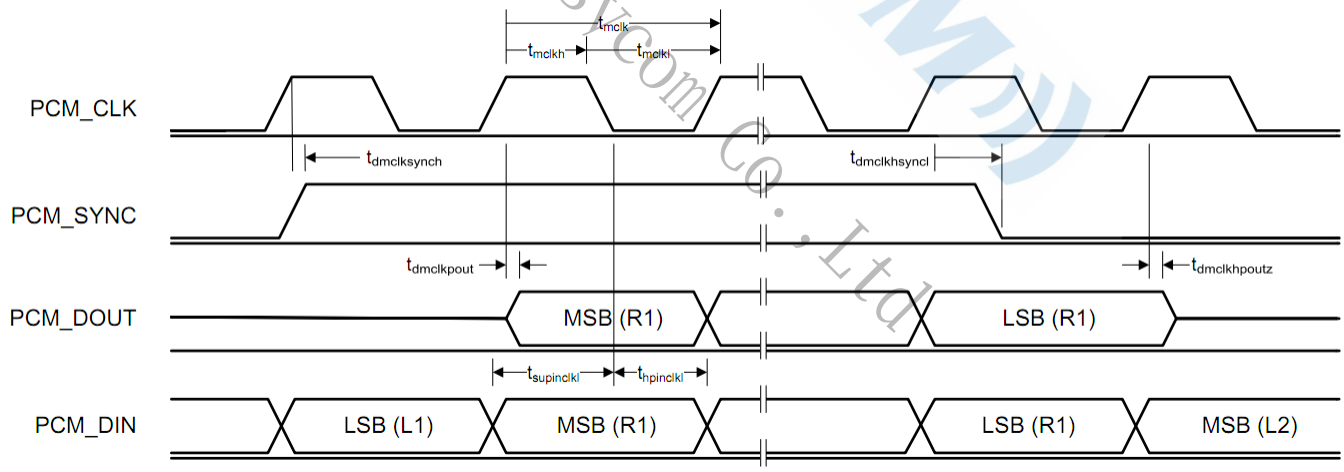

Figure 4-12: Digital audio interface master timing

4.10.5 Digital audio interfaces

Audio digital interfaces include:

- ☐ Digital microphone inputs
- ☐ Standard I²S/PCM interface
- ☐ SPDIF interface
- ☐ Audio MCLK

➢ **Digital microphone inputs**

Up to ten channels of digital microphone inputs are supported. These are grouped as five pairs. Most digital mics can be configured to enable two microphones to share a single data line. **Figure 4-13** shows how FSC-BT1057 supports this mode by outputting data from one microphone on the rising clock edge and from the other microphone on the falling edge of the clock, while otherwise tri-stating their output. Eight digital microphone clock frequencies can be generated. Configurable at: 500 kHz, 571 kHz, 666 kHz, 800 kHz, 1 MHz, 1.33 MHz, 2 MHz, and 4 MHz clock frequencies. The digital microphone function can be assigned to PIOs, see Related Information.

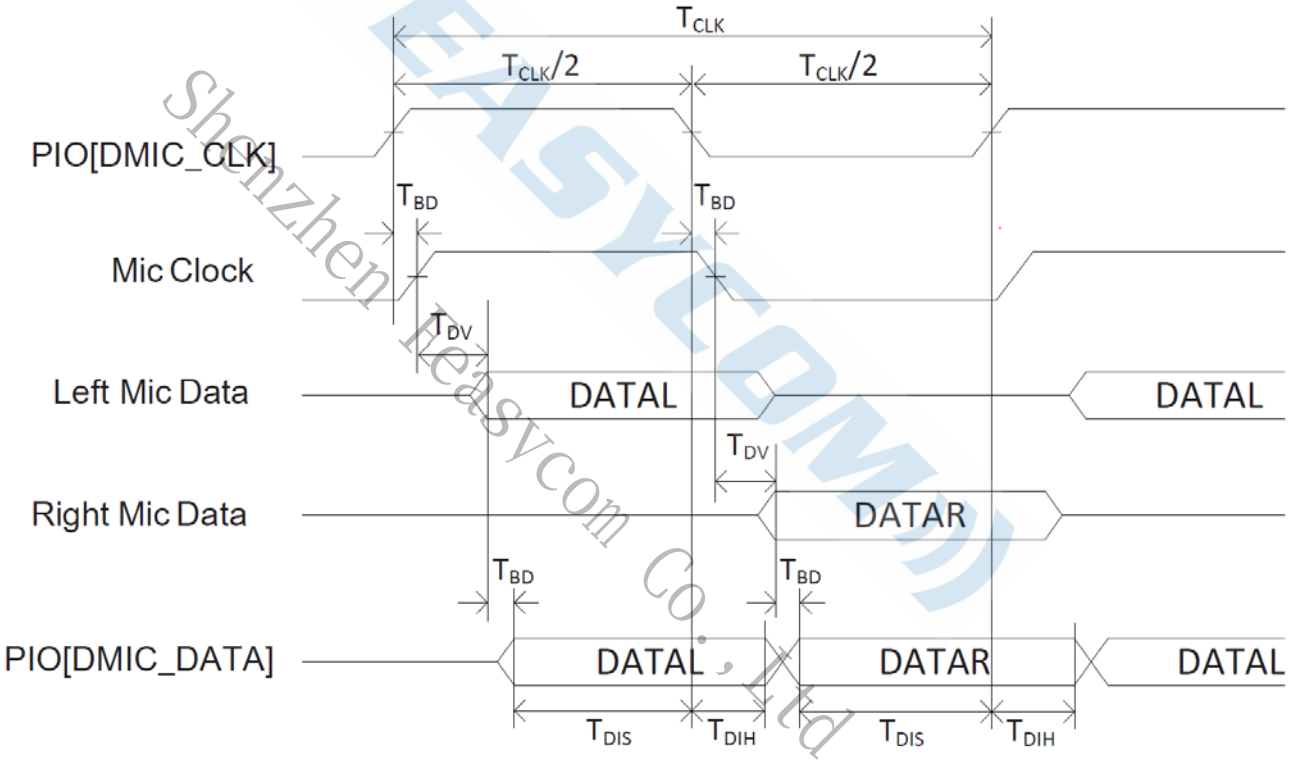

Figure 4-13 Digital microphone timing

Table 4-6 Digital microphone timing parameters

Parameter	Min	Typ	Max	Unit	Description
TCLK	250	-	2000	ns	Clock period
TBD	-	-	-	ns	One-way routing delay from/to FSC-BT1057 to/ from the digital microphone IC
TDV	-	-	-	ns	Delay internal to the digital microphone from the edge of the IC clock to valid data presented by the digital microphone
TDIS	40	-	-	ns	Data Input Setup time
TDIH	0	-	-	ns	Data Input Hold time

4.11 SPDIF interface

SPDIF (IEC 60958) is a digital audio interface. It uses biphase coding to minimize the DC content of the transmitted signal, and enables the receiver to decode clock information from the transmitted signal. FSC-BT1057 has up to two SPDIF interfaces configurable as input or output. These interfaces are compatible with IEC 60958-1, IEC 60958-3, IEC 60958-4, and AES/EBU standards. Signals are input/output via PIO and typically require external line drivers (for 75 Ω cabling) or optical transceivers ('Toslink'). Any PIO is assignable for SPDIF use.

4.12 Audio MCLK

FSC-BT1057 has two internal clock sources for audio interfaces:

- A standard 120 MHz clock (divided down).
- An independent PLL (MPLL) that is usable as an alternate MCLK frequency clock source for the I²S/PCM and SPDIF ports. When it cannot be generated directly from the 120 MHz clock, the MPLL can be output on a PIO for use by an external codec where low jitter I²S/PCM and SPDIF performance is required. **Table 4-7** lists the output frequencies that the MPLL can generate. The MPLL increases system power consumption and therefore only used when necessary.

Table 4-7 Audio MCLK clock output frequencies

MCLK frequency (Hz)	Sample rate (kHz)		
	MCLK ÷ 128	MCLK ÷ 256	MCLK ÷ 384
1,024,000	8	-	-
2,048,000	16	8	-
3,074,000	24	-	8
4,096,000	32	16	-
5,644,800	44.1	-	-
6,144,000	48	24	16
8,192,000	-	32	-
9,216,000	-	-	24
11,289,600	88.2	44.1	-
12,288,000	96	48	32
16,934,400	-	-	44.1
18,432,000	-	-	48
22,579,200	176.4	88.2	-
24,576,000	192	96	-
33,868,800	-	-	88.2
36,864,000	-	-	96
45,158,400	-	176.4	-
49,152,000	384	192	-
67,737,600	-	-	176.4
73,728,000	-	-	192

4.13 Programming and Debug Interface

Important Note:

FSC-BT1057 provides a debug (Pin10~12) interface for programming, updata，configuring, and debugging the FSC-BT1057.

Feasycom provides development and production tools to communicate over the SPI from a PC, although a level translator circuit is often required. All are available from Feasycom.

5. ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

Absolute maximum ratings for supply voltage and voltages on digital and analog pins of the module are listed below. Exceeding these values causes permanent damage.

The average PIO pin output current is defined as the average current value flowing through any one of the corresponding pins for a 100mS period. The total average PIO pin output current is defined as the average current value flowing through all of the corresponding pins for a 100mS period. The maximum output current is defined as the value of the peak current flowing through any one of the correspondin g pins.

Table 5-1: Absolute Maximum Rating

Parameter	Min	Max	Unit
5V (VCHG)	-0.4	+5.75V/6.50 [a]	V
BATTERY (LED 0,1,2)	-0.4	+4.8	V
BATTERY (VBAT_IN)	-0.4	+4.8	V
BATTERY (SYS_CTRL)	-0.4	+4.8	V
VDD_USB/3.3V_OUT	-0.4	+3.8	V
VDD_IO	-0.4	+3.6	V
Other terminal voltages	VSS-0.4	VDD+0.4e3.60 [b]	V
T_{ST} - Storage Temperature	-40	+85	℃

(a) Standard maximum input voltage is 5.75V, a 6.50V maximum depends on firmware version and implementation of over-temperature protection software, for more information contact Feasycom.
(b) VDD is the VDD_IO supply domain for this I/O. Voltage must not exceed 3.6 V on any I/O.

5.2 Recommended Operating Conditions

Table 5-2: Recommended Operating Conditions

Parameter	Min	Type	Max	Unit
5V (VCHG)	4.75 / 3.10 (a)	5	5.75 / 6.50 (b)	V
BATTERY (LED 0,1,2)	1.10	3.70	4.30	V
BATTERY (VBAT_IN)	2.8	3.3	4.30	V
BATTERY (SYS_CTRL)	0	3.3	4.25	V
VDD_USB/3.3V_OUT	2.8	3.3	3.5	V
VDD_IO	1.7	1.8	3.6	V
T_A - Operating Temperature	-40	20	+85	°C

(a) Minimum input voltage of 4.75V is required for full specification, regulator operates at reduced load current from3.1V

(b) Standard maximum input voltage is 5.75V, a 6.50V maximum depends on firmware version and implementation of over-temperature protection software, for more information contact Feasycom.

5.3 Input/output Terminal Characteristics

5.3.1 Digital

Table 5-3: DC Characteristics (V_{DD} - V_{SS} = 3 ~ 3.6 V, T_A = 25°C)

Parameter	Min	Type	Max	Unit
Input Voltage				
V_{IL} - Standard IO Low level input voltage	-	-	0.25 x VDD_IO	V
V_{IH} - Standard IO Low level input voltage	0.625 xVDD_IO	-	-	V
Tr/Tf	-	-	25	nS
Output Voltage				
V_{OL} - Low Level Output Voltage, I_{OL}=4mA	-	-	0.22 x VDD_PADS	V
V_{OH} - High Level Output Voltage, I_{OH}=-4mA	0.75 x VDD_IO	-	-	V
Tr/Tf	-	-	5	nS
Input and Tristate Currents				
Strong pull-up	-150	-40	-10	uA
Strong pull-down	10	40	150	uA
Weak pull-up	-5	-1.0	-0.33	uA
Weak pull-down	0.33	1.0	5.0	uA
C_I Input Capacitance	1.0	-	5.0	pF

5.3.2 Battery Charger

Table 5-4: Battery Charger

Parameter	Min	Type	Max	Unit
Battery Charger				
Input voltage, VCHG	4.75 / 3.10(a)	5.00	5.75 / 6.50(b)	V
(a)Reduced specification from 3.1V to 4.75V. Full specification >4.75V.				
(b) Standard maximum input voltage is 5.75V, a 6.50V maximum depends on firmware version and implementation of over-temperature protection software, for more information contact Feasycom.				
Trickle Charge Mode				
V_{PRE} threshold (rising)	2.0	2.1	2.2	V
V_{PRE} threshold (falling)	1.9	2.0	2.1	V
Trickle charge current: VCHG: 4.25 V to 6.5 V VBAT: 0 V to 2.2 V	1	--	50	mA
Fast Charge Mode				
Charge current during constant current mode, I_{fast} — Max, headroom >0.55V	194	200	206	mA
Min, headroom >0.55V	-	10	-	mA
Reduced headroom charge current, as a percentage of I_{fast} — Mid, headroom =0.15V	50	-	100	%
Charge current step size	-	10	-	mA
V_{float} threshold, calibrated	4.18	4.20	4.22	V
Charge termination current I_{term}, as percentage of I_{fast}	7	10	20	%
Standby Mode				
Voltage hysteresis on VBAT_IN, V_{hyst}	100	-	150	mV
Error Charge Mode				
Headroom(a) error falling threshold	-	50	-	mV

(a) Headroom = VCHG – VBAT_IN

5.3.3 USB

Table 5-5:USB

Parameter	Min	Type	Max	Unit
3V3_USB for correct USB operation(internal)	3.10	3.30	3.60	V
Input Threshold				
V_{IL} - input logic level low	-	-	0.3 x 3V3_USB	V
V_{IH} - input logic level high	0.7 x 3V3_USB	-	-	V

Output Voltage Levels to Correctly Termlnated USB Cable				
V_{OL} - output logic level low	0	-	0.2	V
V_{OH} - output logic level high	2.8	-	3V3_USB	V

5.3.4 LED Driver Pads

Table 5-6:LED Driver Pads

Parameter	Min	Type	Max	Unit
Current, I_{PAD} - High impedance state	-	-	5	uA
Current, I_{PAD} -Current sink state	-	-	50	mA
LED pad voltage, $V_{PAD}I_{PAD}$ = 10mA	-	-	0.55	V
V_{OL} output logic level low[a]	-	0	-	V
V_{OH} output logic level high[a]	-	0.8	-	V
V_{IL} input logic level low	-	-	0.4	V
V_{IH} input logic level high	1	-	-	V

a LED output port is open-drain and requires a pull-up

5.4 Stereo Codec

5.4.1 Analog to Digital Converter

Table 5-7: Analog to Digital Converter (single-ended/differential audio input)

Parameter	Ccnditions		Min	Type	Max	Unit
Resolution	-		-	-	24	Bits
Output Sample Rate, F_{sample}	-		8	-	96	KHz
Input level			-		2.4	V_{pk-pk}
Input impedance	0 dB to 24 dB analog gain			20		KΩ
	27 dB to 39 dB analog gain			10		kΩ
SNR	f_{in} = 1kHz	Single	-	99	-	dBA
	48KHz	differential	-	99	-	dBA
	A-Weighted					
	B/W = 20 Hz to 20 kHz					
	2.4V_{pk-pk} input（0dB gain）					
THD+N	f_{in} = 1kHz	Single	-	-99	-	dB
	48KHz	differential	-	-91	-	dB
	2.4V_{pk-pk} input（0dB gain）					
	B/W = 20 Hz to 20 kHz					
Digital gain	Digital gain resolution = 1/32		-24	-	21.5	dB
Analog gain	3dB steps		-	-	39	dB
Stereo separation (crosstalk)			80			dB

5.4.1 Digital to Analog Converter

Table 5-8: Digital to Analog Converter （differential audio output）

Parameter	Ccnditions			Min	Type	Max	Unit
Resolution	-			-	-	24	Bits
Input Sample Rate, F_{sample}	-			8	-	192	KHz
Output Power(no LPF)	0 dBFS, 10K Ω load					1000	mV
SNR	f_{in} = 1kHz	F_{sample}	Load				
	B/W = 20Hz->20KHz A-Weighted 0dBFS input	48kHz	10KΩ	-	105	-	dBA
THD+N	f_{in} = 1kHz	F_{sample}	Load	-			
	B/W = 20Hz->20kHz 0dBFS input	48kHz	10KΩ	-	-88	-	dB
Digital gain	Digital gain resolution = 1/32			-24	-	21.5	dB
Stereo separation (crosstalk)				80			dB

5.5 Auxiliary ADC

Table 5-9: Auxiliary ADC

Parameter		Min	Type	Max	Unit
Resolution		-	-	10	Bits
Input voltage range(a)		0		1.854	V
Accuracy	INL	-3	-	3	LSB
(Guaranteed monotonic)	DHL	-1	-	2	LSB
Offset		-1	-	1	LSB
Gain error		-1	-	1	%
Input bandwidth		-	100	-	KHz
Conversion time			10		uS

(a) LSB size = 1.854V/1023

5.6 Microphone bias generator

Table 5-10: Microphone bias generator

Parameter	Min	Type	Max	Unit
Output voltage (Tunable, step = 0.1 V)	1.5	-	2.1	V
Output current capability	0.07	-	3.0	mA
DC accuracy	-60	-	60	mV
Crosstalk Between Microphones (Using recommended application circuit)	-	80	-	dB
Load capacitance (From parasitic PCB routing and package	-	-	0.1	nF

6. MSL &ESD Protection

Table 6-1: MSL and ESD

Parameter	Class	Max Rating
MSL grade(with JEDEC J-STD-020)		MSL 3
Human Body Model Contact Discharge per ANSI/ESDA/JEDEC JS-001	2	±2kV(all pins)
Charged Device Model Contact Discharge per JEDEC/EIA JESD22-C101	III	500V (all pins)

6.1 USB Electrostatic Discharge Immunity

FSC-BT1057 has integrated ESD protection on the USB_DP and USB_DN pins as detailed in IEC 61000-4-2.

Table 6-2:USB Electrostatic Discharge Protection Level

IEC 61000-4-2 Level	ESD Test Voltage (Positive and Negative)	IEC 61000-4-2 Classification	Comments
1	2kV contact / 2kV air	Class 1	Normal performance within specification limits
2	4kV contact / 4kV air	Class 1	Normal performance within specification limits
3	6kV contact / 8kV air	Class 2 or class 3	Temporary degradation or operator intervention required
4	8kV contact / 15kV air	Class 2 or class 3	Temporary degradation or operator intervention required

7. RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccate (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the below **Table 7-1** and follow instructions specified by IPC/JEDEC J-STD-033.

Note: The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the below **Table 7-1**, the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccate and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60%RH.

Table 7-1: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated@ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Feasycom surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

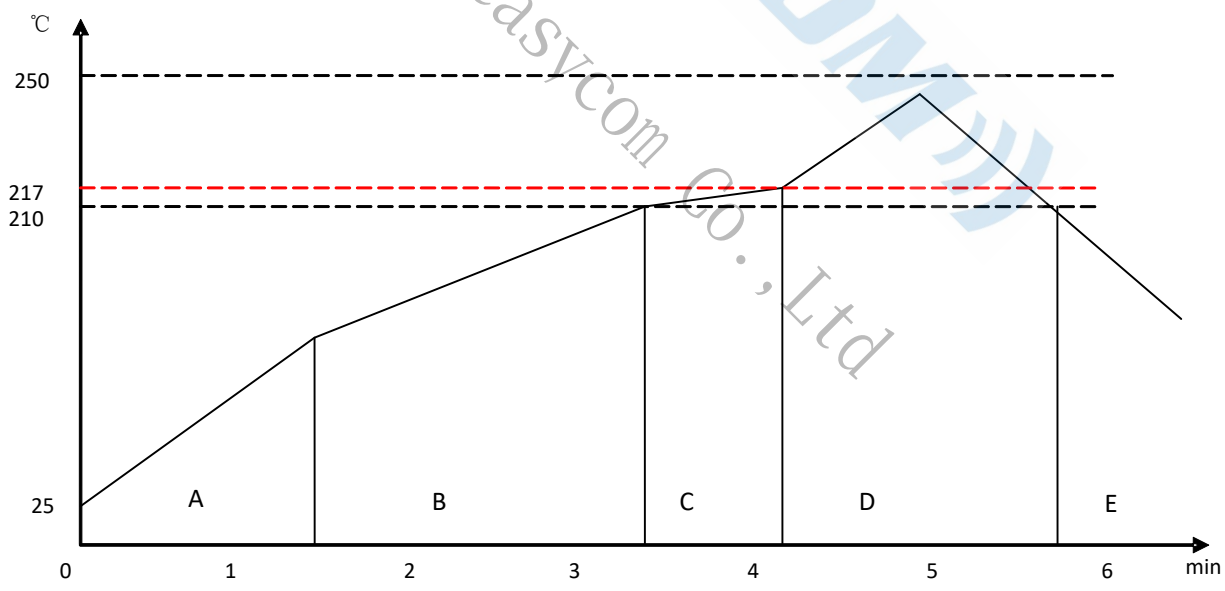

Figure 7-1: Typical Lead-free Re-flow

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB

board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

Equilibrium Zone 2 (C) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

8. MECHANICAL DETAILS

8.1 Mechanical Details

- Dimension: 13mm(W) x 26.9mm(L) x 2.2mm(H) Tolerance: ±0.2mm
- Module size: 13mm X 26.9mm Tolerance: ±0.2mm
- Pad size: 1.6mmX0.6mm Tolerance: ±0.2mm
- Pad pitch: 1.0mm Tolerance: ±0.1mm

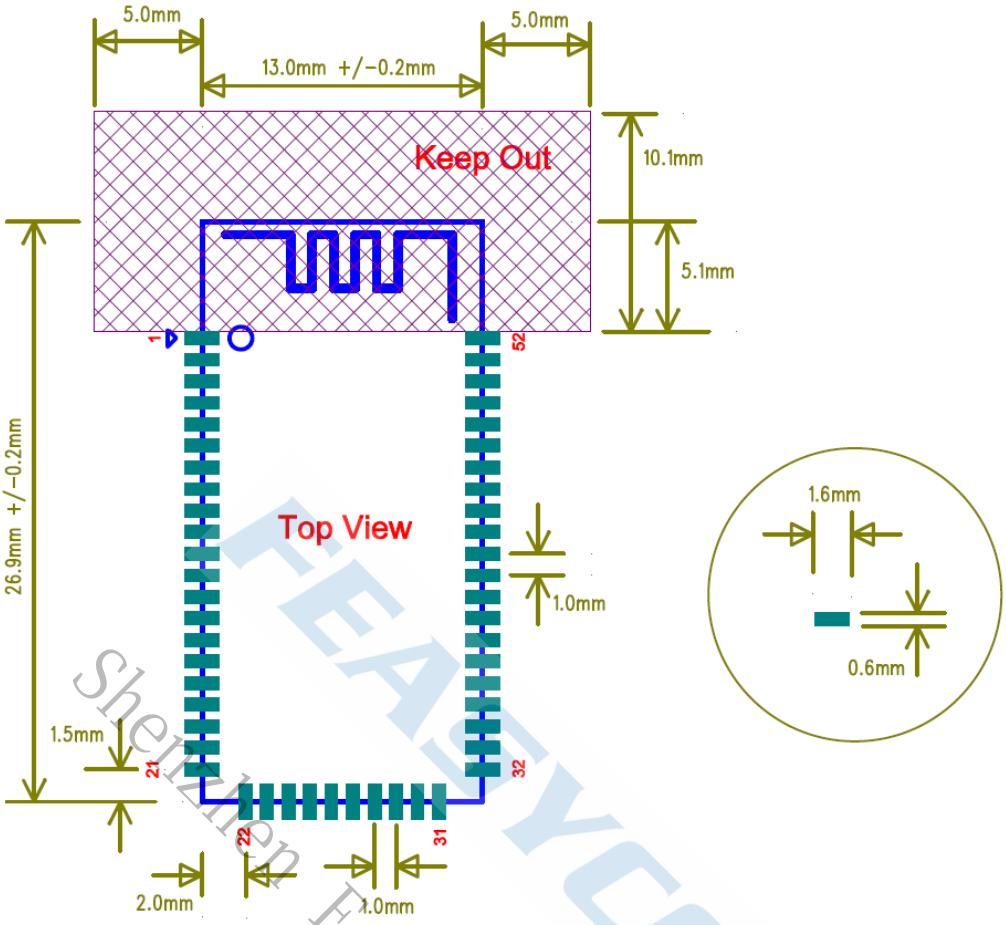

Figure 8-1: FSC-BT1057 footprint

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9. HARDWARE INTEGRATION SUGGESTIONS

9.1 Soldering Recommendations

FSC-BT1057 is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

9.2 Layout Guidelines(Internal Antenna)

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.

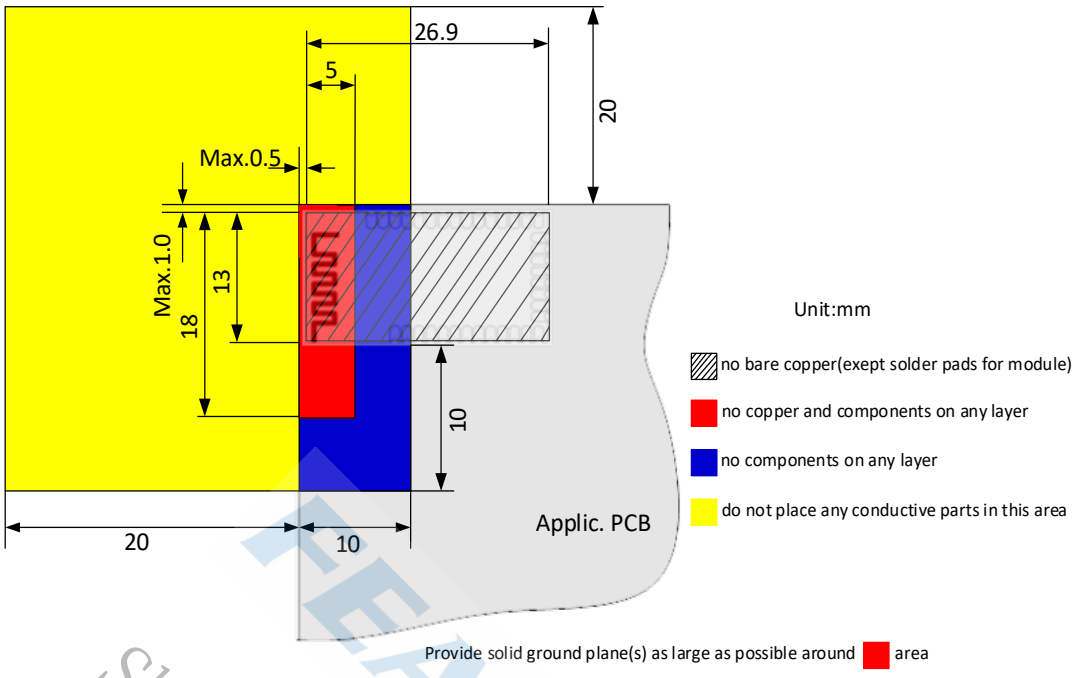


Figure 9-1:FSC-BT1057 Restricted Area

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

9.3 Layout Guidelines(External Antenna)

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in **Figure 9-2** below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

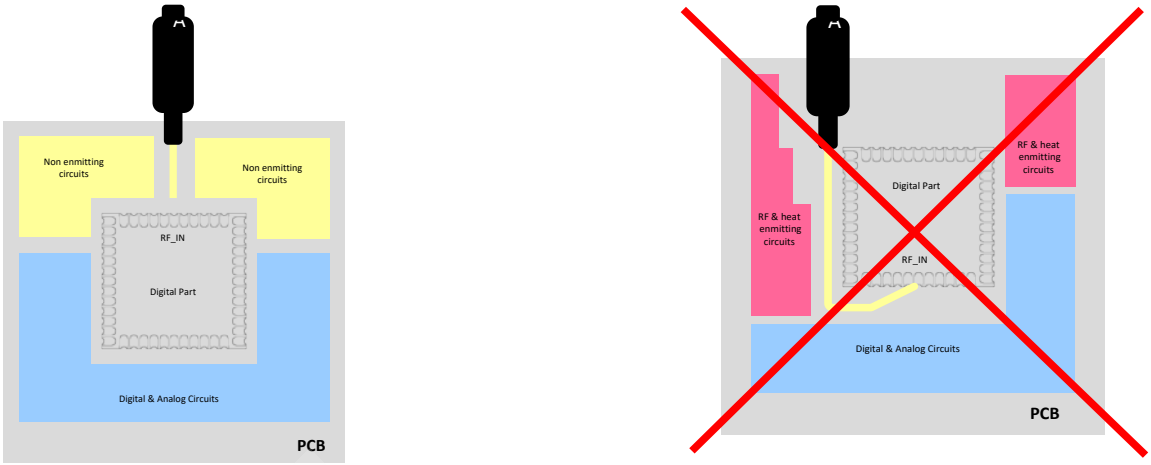


Figure 9-2: Placement the Module on a System Board

9.3.1 Antenna Connection and Grounding Plane Design

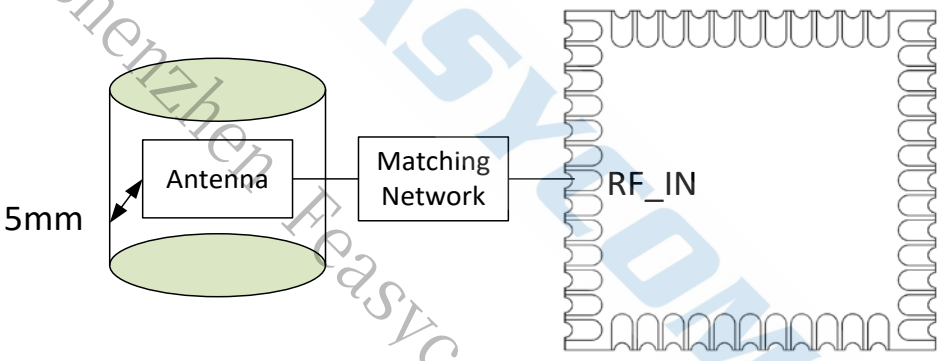


Figure 9-3: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

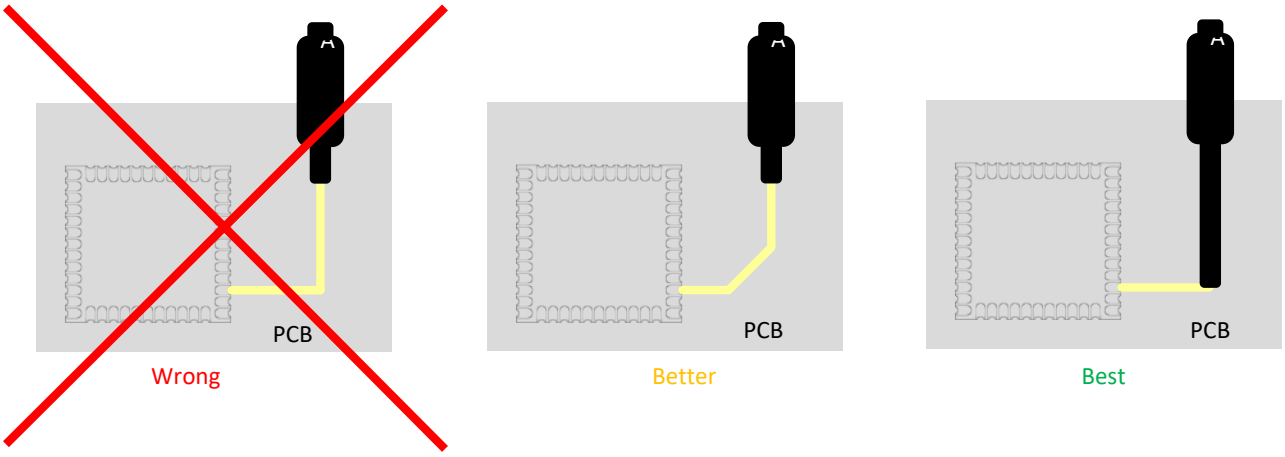


Figure 9-4: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

10. PRODUCT PACKAGING INFORMATION

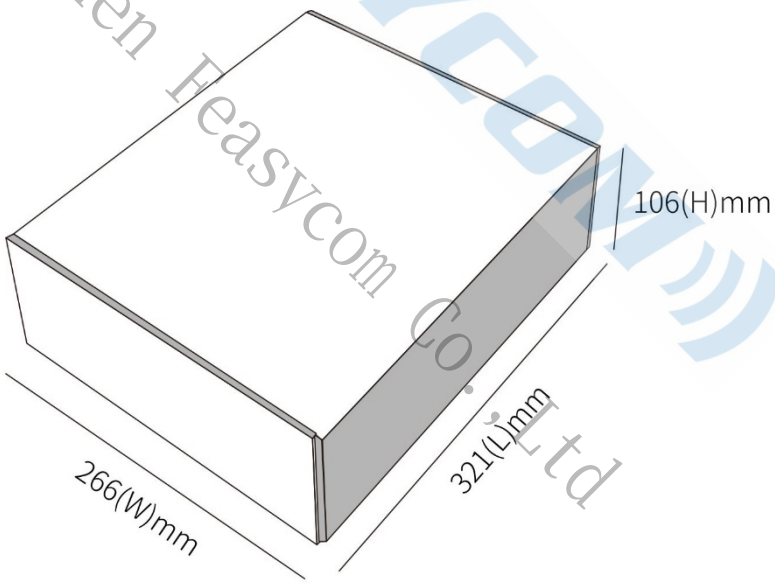
10.1 DefaultPacking

a, Tray vacuum

b, Tray Dimension: 190mm * 175mm

Figure 10-1: Tray vacuum

10.2 Packing box(Optional)



* If require any other packing, must be confirmed with customer

* Package: 1000PCS Per Carton (Min Carton Package)

* The outer packing size is for reference only, please refer to the actual size

Figure 10-2: Packing Box

11. APPLICATION SCHEMATIC